Bruker BioSpin

AVANCE III

IPSO 19" External Unit
Technical Manual

Version 003

think forward

NMR Spectroscopy

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DWG-Nr.: Z4D10607

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Introduction 1

Introduction 1.1

This manual covers the 19“ external spectrometer control unit called Intelligent Pulse Sequence Organizer (IPSO) which are used in AVANCE III spectrometers.

FOR YOUR SAFETY: Read the safety information in this chapter in its entirety before installation and use!

The chapter ***"IPSO Essentials"*** summarizes essential information for users to help them get started quickly and to avoid common mistakes.

The chapter ***"IPSO Organization"*** lists the part/order numbers for the main assemblies, subassemblies and devices.

The subsequent chapters provide more detailed descriptions of assemblies and devices.

Disclaimer 1.2

The unit should only be used for its intended purpose as described in this manual. Use of the unit for any purpose other than that for which it is intended is taken only at the users own risk and invalidates any and all manufacturer warranties.

Service or maintenance work on the unit must be carried out by qualified personnel.

Only those persons schooled in the operation of the AVANCE III should operate the unit.

Read this manual before operating the unit. Pay particular attention to any safety related information.

Safety Issues 1.3

These instructions refer to any IPSO model.

The IPSO may be damaged by inappropriate usage. The damage could be such, that the equipment must not be used before having been checked by a service representative.

The user should recheck the equipment at regular intervals for any damage or wear and is expected to inform the service representative immediately of any abnormality.

WARNING!

Do not use the equipment and inform the service staff, if you are in doubt about the correct state of any component.

In the unlikely case of one of the following, stop using the equipment, disconnect the power supply, report the circumstance to the service staff and ask for instructions:

- The power cord, power plug or power supply are cracked, brittle or damaged.
- Signs of excessive heat are apparent.
- There is evidence or suspicion that a liquid has intruded into any enclosure.
- The power cord or the power supply have been in contact with any liquid.
- The IPSO has been dropped or damaged in any way.
- The equipment does not work correctly.

WARNING!

Do not try to service the equipment by yourself, unless you are specifically asked to do so and are given instructions by the service staff. In case of questions or problems, please contact your nearest Bruker office or representative.

Some components of IPSO can be installed or replaced by the customer. These components are referred to as “Customer Replaceable Units” (CRUs), see ***"Customer Replaceable Units"***.

With the exception of the CRUs, all servicing must be performed by qualified service personnel.

Before maintenance, repair or shipment, the IPSO must be completely switched off and unplugged or disconnected and dismounted from its rack.

Special Safety Symbols *1.4*

These symbols are used on the equipment and/or throughout this manual. They alert to danger and important information:

WARNING!

The symbol indicates a potential risk of injury due to noncompliance to the instructions.

WARNING!

The symbol indicates a potential risk of injury due to contact with high voltage.

WARNING!

The symbol indicates a potential risk of injury due to contact with hot surfaces.

WARNING!

This symbol denotes hints or instructions whose noncompliance could lead to erroneous or incalculable behavior of the system.

Product and Manufacturer *1.5*

The following description refers to:

Product:	IPSO 19“ Unit	P/N H9987
Manufacturer:	Bruker BioSpin GmbH Silberstreifen 4 76287 Rheinstetten Germany	
Conformity:	EN 61010−1	

Intended Use *1.6*

Intended Usage

The IPSO 19“ Unit is to be used only for the limited purpose of controlling the BRUKER AVANCE III spectrometers.

Non−Intended Usage

The IPSO 19“ Units contain generally available computer assemblies and provide their standard interfaces. The IPSO 19“ Unit is not qualified to be used beyond this “Intended Usage” either as a single computer or as part of a network.

Technical Specifications *1.7*

Environmental Requirements

Permissible ambient temperature:	5 to 40 degree celsius.
Permissible altitude:	Up to 2000 meters (above sea level).
Relative humidity:	Max. 80% up to 31 degree celsius and linear decreasing to 50% at 40 degree celsius.
Permissible storage temperature:	5 to 40 degree celsius.
Pollution degree:	2, according to EN 61010−1 or IEC 60664−1 any pollution is non-conductive.
Audible noise:	50 dB.

Utility Requirements for the IPSO−19“ Unit

Ingress protection class:	IP 20, secured against touching dangerous points inside, not secured against ingress of water.
Overvoltage protection category:	CAT II, according to EN61010−1 or IEC60664−1 safe against overvoltage by switching, not safe against lightning.
	Surge immunity of PSU is level 3, according to IEC61000-4-5.
IEC protection class:	Class I, according the IEC 61140, connected to mains by phase, neutral and protective earth.
Input Voltage range:	110/240 V~.
Frequency:	50/60 Hz.
Input Power:	100 VA.
Fuse on mains input:	250 VAC 6.3 A.
Connection:	Socket outlet with phase, neutral and protective earth, according to VDE 0620−1.

Weight and Dimensions of the IPSO 19“ Unit

Weight:	11 kg.
Dimension:	(420 x 532 x 85) mm, according to DIN41494 or IEC 297, (84TE, 2HE)

Preparation and Transportation *1.8*

The IPSO 19“ Unit contains a large amount of sensitive parts and assemblies, therefore it must be handled with care and must not be dropped.

Storage *1.8.1*

If the IPSO is not installed immediately, it has to be inspected for any damage during shipment and must be stored in the original packing.

Attention has to be given to the recommended storage conditions, the temperature and the protection from moisture.

Unpacking *1.8.2*

All packing materials have to be removed. The equipment must be inspected for any damage during shipment.

If damage has occurred during transit, all the shipping cartons should be stored for further investigation. A claim for shipping damage has to be reported immediately.

Installation *1.8.3*

All the requirements concerning the environment described in the ***"Technical Specifications"*** have to be met.

To reduce the risk of electric shock and malfunctioning, install these devices in a temperature controlled and humidity controlled indoor area free of conductive contaminants.

The power supply cord is intended to serve as the disconnect device. The socket outlet should be near the equipment and easily accessible.

The installation of IPSO has to meet all instructions from the “User’s Guide” and in this manual.

Each IPSO model has to be installed in its dedicated rack:

IPSO 19“ Unit: AVANCE CONSOLE WIRED MICROBAY

P/N H03128

Make sure that ventilation and space requirements are according to specification. There must be clearance at the rear for ventilation and at the front for operation.

Make sure that cabling can not be a source of danger.

All cables have to be connected before the IPSO is put into operation.

Operating Instructions 1.9

- Starting up and shutting down the IPSO.
- Operating the users software interface.
- Connecting data interface cables.
- Replacing the Customer Replaceable Units (CRUs).

WARNING!

Except for CRUs, all operations inside the IPSO must be carried out only by a service engineer from the manufacturer or from an agent authorized by the manufacturer.

These operations must be performed according to the instructions in this manual. During any of these operations the user must take the greatest care and perform only the prescribed operations.

Do not operate the equipment in the presence of flammable gases or fumes.

Operator Protection 1.9.1

The electronic circuitry of IPSO is operating with low and safe voltages, except for the power supply and its connection to the mains. Nevertheless, any electrical equipment can become a source of danger under extreme conditions.

WARNING!

Do not loosen, connect or touch any cable during a lightning storm.

Do not use a cable that shows any signs of damage or that has been stressed and could be damaged.

Do not open the IPSO enclosure, except for replacing CRUs.

When opening of the IPSO enclosure is necessary, switch off the unit and let it cool down for five minutes.

Pay attention to the special safety symbols used inside.

WARNING!

Do not open the power supply. There may be dangerous voltage. In case of service, the fan of the power supply can be exchanged without opening the power supply and without opening the IPSO enclosure.

Device Protection *1.9.2*

WARNING!

Always discharge any static electricity from yourself before touching uncovered metal, electronic devices or connectors from the PCB!

Do not connect a receiver to the LVDS connector of the controller in Slot 2 of the IPSO 19” Unit. There data will never be valid.

A LVDS cable should never be removed from or connected to a powered controller. Corrupted data could be sampled as valid.

Do not connect more than one gradient amplifiers to the same system.

Customer Replaceable Units *1.9.3*

To insert and remove a Customer Replaceable Unit (CRU), follow the instructions in this manual.

Replacing CRUs requires opening of the enclosure. Before doing this, the unit must be completely switched off and unplugged or disconnected and dismounted from its rack.

The following replaceable units are available with the IPSO 19“ Unit:

- IPSO-Tx-controller Board P/N H12538F2
- IPSO-Rx-controller P/N H12532
- PC 2CH RS232 PCI Adapter P/N O10394
- PCI Rx-controller P/N H12565
- DPP1 Digital Preemphasis Board P/N H12513F1
- RTC Battery 3V Lithium P/N 72385, type “Varta CR2032”

Maintenance and Cleaning 1.10

Cleaning 1.10.1

Cleaning the surface of the enclosure and/or front panel can be carried out by the customer, but the following instructions must be adhered to.

1. Switch off the equipment and unplug the power cable and all data cables.

WARNING!

Use only water or a mild detergent. The surface might be damaged or etched, if solvents were to be used.

2. Clean up the surface with a dry or damp cloth.
3. Let the enclosure completely dry before installing.
4. Reconnect all cables and power up.

Maintenance 1.10.2

The IPSO can be expected to have a long and trouble-free life with a minimum of preventive maintenance. Environmental issues are essential in determining the reliability. The temperature and humidity have to be within specifications. The area around the unit should be kept clean and dust free.

With the exception of the CRUs, all servicing must be performed by qualified service personnel.

Before maintenance, repair or shipment, the unit must be completely switched off and unplugged or disconnected and dismounted from its rack.

Service Requests 1.10.3

In case of questions or problems, please contact your nearest Bruker office or representative. A list of all our offices is published on the Bruker website at www.bruker.com.

Terms and Abbreviations *1.11*

TOPSPIN PC	Processing computer running TOPSPIN; server for the IPSO diskless Linux.
IPSO	Intelligent Pulse Program Organizer; System consisting of the IMB, the PCI host and a different bundle of controllers.
IPSO 19” Unit, IPSO 19-inch Unit	IPSO version as standalone case of the 19“ standard.
IPSO Host, CCU, PCI Host, spect	Assembly group containing the IPSO Host Controller (PC module, ETX), computer interfaces and the host bus (PCI).
IPSO Host Controller	IBM−PC compatible module computer (ETX).
IPSO Motherboard, IMB	IPSO host for the IPSO 19” unit, including computer, interfaces and bus structure.
IPSO−Tx, Tx-controller, TxCtrl	Tx-controller, capable of sending sequences of application parameters; Single channel for IPSO 19” Unit.
IPSO−Rx, Rx-controller, RC, rc R−Controller, RxCtrl.	Rx-controller, capable of receiving sequences of application results or parameter streams sent by TxCtrl in cases of using the “ipsotest”.
T−Controller, TC, tc; F−Controller, FC, FC1, fc, fc1; G−Controller, GC, gc	Tx-controller with dedicated and application specific functionality for: T = Timing control, F = Frequency control, G = Gradient control; In print messages: “...F−controller1, (fc1)...” means the first channel frequency controller.
X−Controller, XC, xc Controller Board, Controller	Collective term of controllers without functional differentiation; means in each case a TC or RC controller based on C6400.
U−Controller, UC, uc	Stands for “unknown controller” and describes a C6400 based controller with unknown content in its version register, e.g. a C6400−based device of an unknown manufacturer.
C6400	CPU of the controller; DSP from Texas Instruments.
IMB	IPSO motherboard, IPSO host for the 19” Unit.
Host−Bus, PCI−Bus	Control, data, and address bus for communication between Host Controller and X−Controllers.
RCP	Real-time Clock Pulse.
LVDS Cable	Transmission cable at the LVDS connector of X−controllers.
PCI−Master	PCI device which is able to initiate a transaction over the PCI bus (host bus).
Local Address	Onboard address out of the local processor’s address layout, different from the PCI address in the upper 10 bit.

PCI Address	Onboard address out of the PCI bus address layout, different from the local address in the upper 10 bit; The Bruker user interfaces use the local address only.
Channel	Controller dedicated to a sub-task of the application.
AQ Bus	Bundle of signals which control on a clock base (80 MHz) the channel operation and the communication between the channels.
Master Controller	Controller of the zero delay channel (first one) which decides on the AQ bus operation and communicates with the slave controllers. One exclusive master has to be in the system. Only the master drives many of the AQ bus signals.
Slave Controller	A controller which is functionally dependent on the decisions of the master controller. “Slaves” have a clock cycle delay with respect to the master of >/= 0 It is not allowed to have only slave controllers in the system.
Last Slave Controller	Is the slave with the greatest delay in the system respective to the master. Only this Slave drives some AQ bus signals and communicates with the master.
Independent Controller	Whenever started runs its own program independent of the AQ bus. The independent controller drives no AQ bus signals. It is not allowed to have only independent controllers in the system.
Trigger, trigger event, external event	External signal which can assign the time of any decision to the master controller.
Firmware	Software which is loaded to the controller memory and runs the C6400.
AQ device driver	A program that must be loaded into the Linux Kernel which enables access to the X-controllers.
AQSTART	Start of application; carried out via the T-controller and AQ Bus.
semif	Register to select FIFO or C6400 to load the LVDS output.
EDMA, QDMA	Transactions of data between memory ranges and/or interfaces initiated by the DMA controller of C6400; EDMA = Extended DMA, QDMA = Quick DMA (not faster than EDMA).
OPT, SRC, CNT, DST, IDX, RLD	Fields of the DMA controllers: Option, Source, Count, Destination, Index, Reload.
EMIFA, EMIFB	Interfaces of the C6400 to the memory and registers; EMIFA = 64-bit, EMIFB = 16-bit.

IPSO Essentials 2

Structure and Features 2.1

Features 2.1.1

- IPSO is a digital spectrometer control unit with a variable number of output channels (Tx-controllers).
- Each Tx-controller outputs a stream of 48-bit words at a clock rate of 80 MHz per word.
- Transferal of a complete set of frequency parameters requires two words.
- The time resolution of parameter switching in any combination of frequency, Phase, Amplitude is 12.5 ns.
- The minimal duration of any combination of parameters is 25 ns.
- Gradient channels require one word per gradient.
- The maximal number of addresses for different gradients (the maximum number of gradient channels) is 1k.
- A constant time delay between the outputs of the different Tx-controllers may be adjusted to any number of 80 MHz clock cycles up to 2^{29} x 12.5 ns.

Structure 2.1.2

The distinctive parts of the system are:

- The host controller which handles administrative tasks.
- A number of Tx-controllers for generating and transferring the parameter sequences.
- The sequencer which provides a means of communication between the Tx-controllers.

The Controllers

The system contains the 3 types of controllers:

- Host controller
- Rx-controller
- Tx-controller.

Host Controller

There is only one host controller in the system. The host controller is an IBM compatible PC with all standard interfaces thus making access possible to the whole pool of standard hardware and software.

The host controller boots its operating system software (diskless LINUX) from and communicates with the TOPSPIN PC over Ethernet. It also communicates over its standard interfaces with the Rx- and the Tx-controllers and with peripheral devices.

Rx-controller

The Rx-controller is able to receive 48-bit words at its LVDS interface at a rate of up to 100-Mega words. Therefore it can be used as a fast data link from the receiver channel to the transmit channel, bypassing the ethernet and the TOPSPIN PC. Furthermore all Tx-controllers and their LVDS interfaces can be tested with the IPSOTEST if their interfaces are connected to a Rx-controller.

Real-time processing of that data can be done by an onboard DSP. The processed data can be transferred by the DMA channels of the DSP over the system bus to any other controller or may be fetched by any other controller.

Usually there is one Rx-controller in the system. Without additional software (that means transparent to the software) it is possible to include additional Rx-controllers using extension boxes.

The Rx-controller has no connections to the Sequencer and communicates and exchanges data with other controllers via the system bus. It will function in any slot of the IPSO but should be inserted in slot 1.

Tx-controller

Depending on its configuration, the Tx-controller can be used for any of the 3 output functions in the system. These functions are the T-controller servicing the RCP outputs at T0 with timing signals, the F-controller generating the frequency parameters for the SGUs and the G-controller generating the gradient packets for the amplifiers.

The Tx-controllers and their common sequencer are the most decisive parts of the IPSO system. The sequencer is a single device, just one piece of silicon. It contains the communication and decision making logic of all Tx-controllers and the communication bus between them known from former systems as the AQ-bus. The AQ-bus allows for real time communication on a 1-clock base of 12.5 nsec.

The controller itself consists of a DSP with memory, FIFO, output logic and interfaces to the system bus and the Sequencer. The DSP gets its code from the Host Controller, generates the parameter sequences and writes them into the FIFO. Its most important task is to keep the FIFO full. The Sequencer (once started) reads the words out of the FIFOs of all controllers, realizes the defined timing in each channel and controls the outputs.

The global functions of the sequencer (e.g. START, STOP, SUSPEND, RESUME and so on) are part of the sequencer logic of the T-controller. Therefore a T-controller has to be in the system to carry out any type of acquisition.

LVDS

The LVDS cable is the transport media for digital data words between the Tx- and the Rx-controllers respectively and the peripheral devices like SGU, gradient amplifier, DRU and DPP (Digital Preemphasis Processor). The abbreviation LVDS means “Low Voltage Digital Signal”. The voltage switching range of the data lines is between 1.0 V and 1.4 V.

The devices used take 48-bit data words at a clock rate of 80 MHz (and 100 MHz between DRU and Rx-controller respectively) and serialize and transport them over 8 balanced data line pairs accompanied by one clock pair. At the receiver side the data stream is deserialized and the 48-bit data word and its 80 MHz clock are reconstructed.

Because there are 8 data lines, the cable has to transport 6 data bit plus one balance bit per 12.5 nsec. That means a bit frequency of 560 MHz on each data line. Since a good signal quality needs a good transmission behavior up to the fifth harmonic wave this cable has to transport the signals up to about 3 GHz without frequency dependent distortions.

The LVDS cable driver is always active even if the Tx-controller is transmitting no valid data.

There are 2 options called “Deskew” and “Preemphasis” which are intended to compensate the negative influence of cables longer than about 3 meters to the signal quality. The normal cable length of under 2 meters requires neither Deskew or Preemphasis.

Deskew

This feature minimizes the effective skew of the different data line pairs in the cable. To be effective it has to be enabled at the receiver and carried out at the transmitter. The default state at introduction is “NOT ENABLED” at the receiver and is activated at the transmitter by a software command only.

If enabled at the receiver Deskew has to be carried out after power-up and again each time after the cable has been unplugged or plugged in under power. This can be done through the software using the IPSOTEST program command “Deskew”. Software activated Deskew needs TOPSPIN 2.0b6 and a Tx-controller with P/N H12538F2. Otherwise with “Deskew enabled at the receiver” the system has to be powered up again after reconnecting.

Preemphasis

This feature compensates for the greater need of charge on cables longer than 2 meters. To be effective it needs one cable length dependent resistor at the transmitter.

The state of the Tx-controllers with part number “H15538” and ”H15538F1” and H12538F2 is “NO PREEMPHASIS”

Besides the data and clock lines the LVDS cable includes 4 lines of an USB channel (currently not used) and 2 state lines. The state lines tell the Tx-controller the type of device that is connected, for example “unconnected, SGU connected, gradient amplifier connected, DPP connected”.

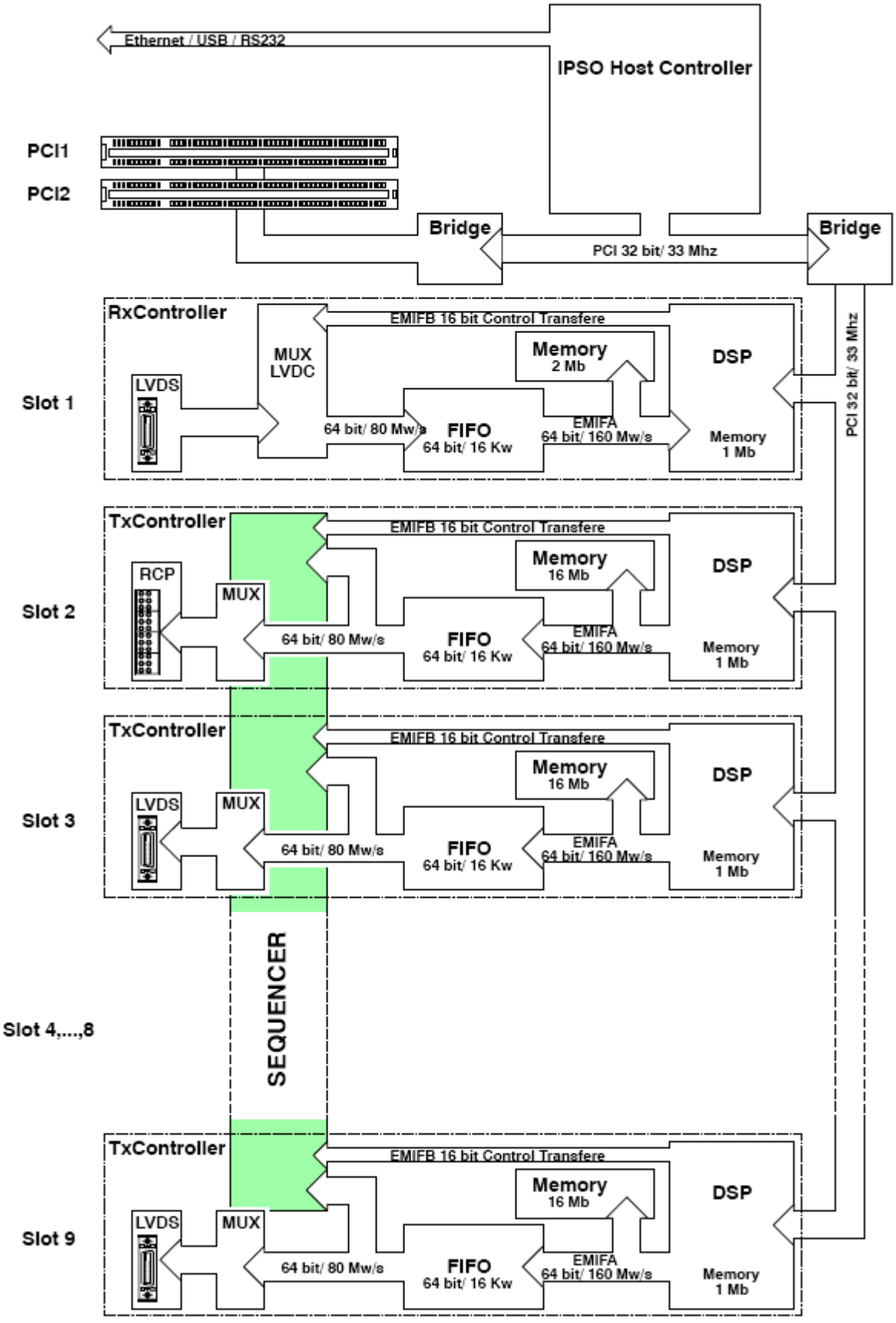

Ethernet / USB / RS232
IPSO Host Controller
PCI1
PCI2
Bridge
PCI 32 bit/ 33 Mhz
Bridge
PCI 32 bit/ 33 Mhz
RxController
EMIFB 16 bit Control Transfere
MUX
LVDC
Memory
2 Mb
DSP
LVDS
Slot 1
64 bit/ 80 Mw/s
FIFO
64 bit/ 16 Kw
EMIFA
64 bit/ 160 Mw/s
Memory
1 Mb
TxController
EMIFB 16 bit Control Transfere
Memory
16 Mb
DSP
RCP
MUX
Slot 2
64 bit/ 80 Mw/s
FIFO
64 bit/ 16 Kw
EMIFA
64 bit/ 160 Mw/s
Memory
1 Mb
TxController
EMIFB 16 bit Control Transfere
Memory
16 Mb
DSP
LVDS
MUX
Slot 3
64 bit/ 80 Mw/s
FIFO
64 bit/ 16 Kw
EMIFA
64 bit/ 160 Mw/s
Memory
1 Mb
SEQUENCER
Slot 4,...,8
TxController
EMIFB 16 bit Control Transfere
Memory
16 Mb
DSP
LVDS
MUX
Slot 9
64 bit/ 80 Mw/s
FIFO
64 bit/ 16 Kw
EMIFA
64 bit/ 160 Mw/s
Memory
1 Mb

Figure 2.1: Block Diagram of the IPSO 19" Unit

Handling 2.2

Electrostatic Discharge 2.2.1

WARNING!

Always discharge any static electricity from yourself before touching uncovered metal, electronic devices or connectors from the PCB!

Boot Procedure 2.2.2

The IPSO needs to boot its diskless LINUX from the TOPSPIN PC via the Ethernet. This connection with or without an hub included requires the following cable:

Connection	Type	Color	Part Number	Length
Point-to-point	UTP/CAT5, crossed	red	84338	5 meters
			83980	10 meters
Point-to-hub	UTP/CAT5, straight	white	83025	5 meters
			83026	10 meters

If connected, the IPSO needs only to be switched on or to be reset to begin booting.

Power ON/OFF Button

Press the button for about 2 seconds to switch the system on and 6 seconds to switch it off.

Reset Button

This button resets the host controller, the PCI logic and restarts the boot process.

Opening the IPSO 19” Unit

The case of the IPSO has to be opened to facilitate controller/PCI card installation. To do that it is only necessary to remove the two screws (right and left) on the top cover next to the front side.

Rules of Modularity on the IPSO 19” Unit

There are two kind of controllers (Rx-controller and Tx-controller) which can be plugged into the 9 slots. Some of the slots are dedicated to a unique controller and some stamp a special function on the generic Tx-controller:

Rx-controller:	The Rx-controller should be used in **slot 1**. In any other slot it can only be used as a receiving controller.
Tx-controller:	Slots 2 to 9 have been designed for the Tx-controllers. When plugged into slot 1 the Tx-controller would be recognized as “unknown” (U-controller). In this case it will not be able to communicate with the sequencer and to transmit data.
Slot 2:	This is the only slot that provides access to the acquisition global functions like START, STOP and so on and to the RCP outputs. Therefore the Tx-controller in this slot receives the task of the Timing Controller (T-controller). It controls the RCP outputs instead of its LVDS output. Do not connect a cable to this LVDS connector. The LED below this connector is always off.
Slot 3 to Slot 9:	Tx-controllers in these slots will work as default as a Frequency Controller (F-controller) or a Gradient Controller (G-controller). The LED below the LVDS connector lights green at the F-controller and yellow at the G-controller. The channel numbering for the F-controller begins at the left most one and counts upwards to the right. No gap is allowed between the F-controllers.

Which Frequency Controller will become the Gradient Controller?

Only the F-controller which is connected to a gradient amplifier will be configured as a G-controller. In this case its LED below the LVDS connector will change from green to yellow.

Connecting more than one controller to a gradient amplifier is not supported by TOPSPIN.

Prior to Release 2.0, TOPSPIN will only allow the last F-controller of a system to become the G-controller. This would be the last one on the right side of the IPSO 19” Unit.

Currently an arbitrary F-controller can be selected as G-controller if all higher numbered F-controllers are logically disabled. In the future a later release might advantageously allow the G-controller to be freely selected by connecting the gradient amplifier.

For Example:

Three F-controllers and one G-controller in the slot of Fx-controller 4 are used.

If you want to disable the present G-controller and use Fx-controller 3 instead, you have to:

1. Unplug the LVDS cable from previous G-controller.
2. Plug the LVDS cable to Fx-controller 3.
3. Login to IPSO as root.
4. Run: root@IPSO:/opt/test>sh aqmod.sh -disable fctrl4.

Ports 2.3

The IPSO services the following input and output ports:

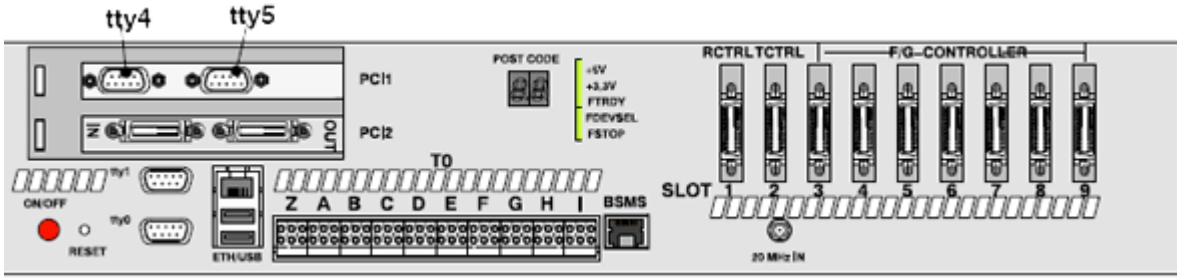


Figure 2.2: Front View of IPSO 19" Unit

PCI Slots 2.3.1

The two standard PCI slots meet the PCI Local Bus Specification Revision 2.1. Both slots are intended for 5-volt signaling cards (IPSO AQS can accept short cards only).

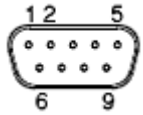
The total power consumption, summarized for both slots, must not exceed the following values:

IPSO 19" Unit: 10A from +5V and 3.5A from 3.3V

Connectors *2.3.2*

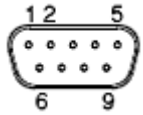
tty0, tty1: RS232C on ETX module, maximum baud rate 115.2 K baud The configuration of the tty-interfaces (parity, number of stop bits, kind of handshake, baud rate) is defined and set by the application program.

The type of connector is D-Sub, 9-pin, female

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal	
1	RI	4	DTR	7	RTS	
2	RxD	5	GND	8	CTS	
3	TxD	6	DSR	9	not connected	

tty4, tty5: RS232C on auxiliary PCI adapter EX-41052, max. baud rate 115.2Kbaud The configuration of the tty-interfaces (parity, number of stop bits, kind of handshake, baud rate) is defined and set by the application program.

The type of connector is D-Sub, 9-pin, female

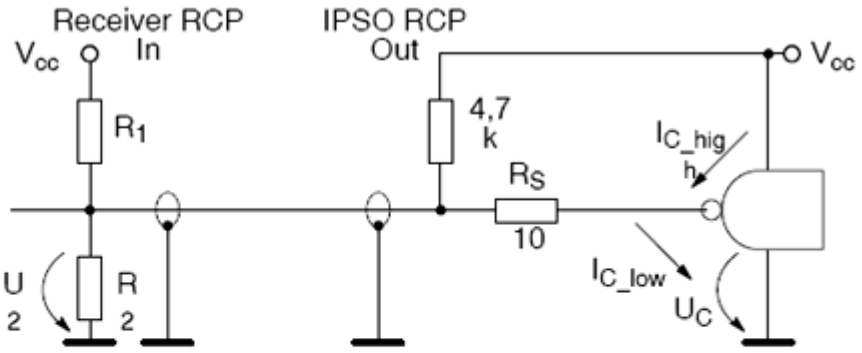
Pin Number	Signal	Pin Number	Signal	Pin Number	Signal	
1	CDC	4	DTR	7	RTS	
2	RxD	5	GND	8	CTS	
3	TxD	6	DSR	9	RI	

ETH 10/100 Base T, Intel 82551ER

USB USB 1.1 OHCI

Electrical Properties and Constraints of the RCP Outputs and Receiver Inputs

The high and low switching levels (U2) and the associated current (IC) of the RCP signals depend on the circuitry and driving capacity of the driver and the circuitry of the connected receiver.



$V_{CC} = 5V$

$U_{C\_low} = 0,3V$

$U_{C\_high} = (3,0..3,3)V$

$$U_{2\_low/high} = \frac{\left\{V_{CC} + U_{C\_low/high}\left(\frac{R_1}{R_S}\right)\right\}}{\left\{1 + \frac{R_1}{R_2} + \frac{R_1}{R_S}\right\}}$$

$$I_{C\_low/high} = \frac{\left\{U_{2\_low/high} - U_{C\_low/high}\right\}}{R_S}$$

Figure 2.3: RCP Circuit

The following table shows the resulting voltage levels and currents for some combinations of R1/R2. Other combinations are possible and can be checked by the formulas above.

Table 2.1: RCP Voltage Levels and Currents

Parameter	Combinations of Input Circuit				Units
R_1	100	100	100	200	Ohm
R_2	68	-	100	200	Ohm
U_2 if I_c=0	2.0	5.0	2.5	2.5	V
U_{2_low}	0.64	0.73	0.66	0.5	V
U_{2_high}	2.8	3.18	2.91	2.95	V
I_{c_low}	34	43	36	20	mA
I_{c_high}	-20	-12	-30	-25	mA

IPSO 19“ Unit

The signals which are available at the front side connector T0 are:

Type of Signal	Direction	Name	Count
RCP Output	Out	TCU_xy	51
Trigger Input	In	Trig 1...4	4
External Suspend	In	EXT_MAN_SUSP	1
External Stop	In	EXT_MAN_STOP	1
Emergency Stop	In/Out	EX_SGU_RES	1
Peripheral Status	In	SGU_ST	1
Next Value Clock for Preemphasis	Out	EXT_GCLK	1

Other 19 RCP signals (red shadowed in column “T0”) are available at connector ST47 inside of the IPSO case.

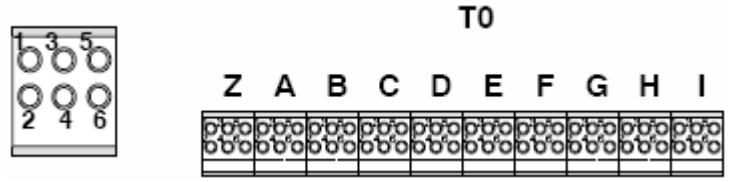


Figure 2.4: RCP Pin Location of IPSO 19” Unit

Table 2.2: Pin Assignment of the RCP Signals on IPSO 19“ Unit

Source Destination	FIFO Word + Bit Position (64..1)		tctrl Output reg. tout0...tout 4	Set nmr 0 (#)	Set nmr 3 (#)	Set nmr 4 (#)	Layout Name	Direction	NMR		
	A	B							Meaning	T0	BSMS
BSMS/LCB		2	T0(0)		0		TCU62	out	!LOCK_HOLD	B1	2
BSMS/SCBR		3	T0(1)		1		TCU0	out	!HOMOSPOIL	B2	6
1H Transm.		4	T0(2)		2		TCU1	out	SELH_!H/F	B4	
1H Transm.		5	To(3)		3		TCU2	out	SELX_!X/F	B5	
BSMS/LCB		6	T0(4)		4		TCU3	out	!INT_A_(Z0)	B3	4
BP		7	T0(5)		5		TCU4	out	MIXCC	B6	
		8	T0(6)		6		TCU5	out	res	C1	
HPPR		9	T0(7)		7		TCU6	out	RCP_PA_SWITCH	C2	
QNP		10	T0(8)		8		TCU7	out	FXA	C3	
QNP		11	T0(9)		9		TCU8	out	FXB	C4	
		12	T0(10)		10		TCU9	out	res	D1	
		13	T0(11)		11		TCU10	out	res	D2	
		14	T0(12)		12		TCU11	out	res	D3	
		15	T0(13)		13		TCU12	out	res	D4	
		16	T0(14)		14		TCU13	out	res	D5	
		17	T0(15)		15		TCU12	out	res	D6	
		18	T1(0)		16		TCU15	out	res	G1	
		19	T1(1)		17		TCU16	out	res	G2	
		20	T1(2)		18		TCU17	out	rest	G3	
		21	T1(3)		19		TCU18	out	res	G4	
		22	T1(4)		20		TCU19	out	res	G5	
		23	T1(5)		21		TCU20	out	res	G6	
		24	T1(6)		22		TCU21	out	res	H1	

Source Destination	FIFO Word + Bit Position (64..1)		tctrl Output reg. tout0...tout 4	Set nmr 0 (#)	Set nmr 3 (#)	Set nmr 4 (#)	Layout Name	Direction	NMR		
	A	B							Meaning	T0	BSMS
		25	T1(7)		23		TCU22	out	res	H2	
MED		26	T1(8)		24		TCU23	out	ECG_START_TRIG	H3	
MED		27	T1(9)		25		TCU24	out	AUT_TUNG_IN	H4	
MED		28	T1(10)		26		TCU25	out	AKTIV_DEC_RES	H5	
MED		29	T1(11)		27		TCU26	out	AKTIV_DEC_RES	H6	
MED		30	T1(12)		28		TCU27	out	Customer specific	I1	
MED		31	T1(13)		29		TCU28	out	Customer specific	I2	
MED		32	T1(14)		30		TCU29	out	Customer specific	I3	
MED		33	T1(15)		31		TCU30	out	Customer specific	I4	
		34	T2(0)			0	TCU31	out	GAIN_0_TR1	ST47 pin 1	
		35	T2(1)			1	TCU32	out	GAIN_2_TR1	ST47 pin 3	
		36	T2(2)			2	TCU33	out	C/AB_TR1	ST47 pin 5	
		37	T2(3)			3	TCU34	out	GAIN_0_TR2	ST47 pin 7	
		38	T2(4)			4	TCU35	out	GAIN_1_TR2	ST47 pin 9	
		39	T2(5)			5	TCU36	out	GAIN_2_TR2	ST47 pin 11	
		40	T2(6)			6	TCU37	out	GAIN_2_TR1	ST47 pin 13	
1H 1KW AMPL		41	T2(7)			7	TCU38	out	RELAY_H	E3	
X 1KW AMPL		42	T2(8)			8	TCU39	out	RELAY_X	E4	
X 1KW AMPL		43	T2(9)			9	TCU40	out	RELAYH	E5	
		44	T2(10)			10	TCU41	out	res RACK_ON/OFF	E6	

Table 2.2: Pin Assignment of the RCP Signals on IPSO 19“ Unit

Source Destination	FIFO Word + Bit Position (64..1)		tctrl Output reg. tout0...tout 4	Set nmr 0 (#)	Set nmr 3 (#)	Set nmr 4 (#)	Layout Name	Direction	NMR		
	A	B							Meaning	T0	BSMS
		45	T2(11)			11	TCU42	out	RCP	F1	
X 1KW AMP		46	T2(12)			12	TCU43	out	RELAY Z	F2	
		47	T2(13)			13	TCU44	out	RCP_Scope	F3	
		48	T2(14)			14	TCU45	out	RCP_EXT_DEV	F4	
		49	T2(15)			15	TCU46	out	RCP	F5	
High Power		50	T3(0)			16	TCU47	out	STP1_DIR	ST47 pin 15	
High Power		51	T3(1)			17	TCU48	out		ST47 pin 17	
High Power		52	T3(2)			18	TCU49	out		ST47 pin 19	
High Power		53	T3(3)			19	TCU50	out		ST47 pin 21	
High Power		54	T3(4)			20	TCU51	out		ST47 pin 23	
High Power		55	T3(5)			21	TCU52	out		ST47 pin 25	
High Power		56	T3(6)			22	TCU53	out		ST47 pin 27	
High Power		57	T3(7)			23	TCU54	out		ST47 pin 29	
2H Lock Switch		58	T2(8)			24	TCU55	out	SEL_2H AMP and TUNE_MODE in MRIs only	A1	
		59	T3(9)			25	TCU66	out	res	ST47 pin 31	
		60	T3(10)			26	TCU57	out	res	Z2	
		61	T3(11)			27	TCU58	out	Q_SWITCH and SCO/CCO in MRIs only	A3	
		62	T3(12)			28	TCU59	out	SEL_1X/2H and REF_MODE in MRIs only	A2	
		63	T3(13)			29	TCU60	out	res	F6	

Table 2.2: Pin Assignment of the RCP Signals on IPSO 19“ Unit

Table 2.2: Pin Assignment of the RCP Signals on IPSO 19“ Unit

Source Destination	FIFO Word + Bit Position (64..1)		tctrl Output reg. tout0...tout 4	Set nmr 0 (#)	Set nmr 3 (#)	Set nmr 4 (#)	Layout Name	Direction	NMR		
	A	B							Meaning	T0	BSMS
		64	T3(14)			30	TCU61	out	res	I5	
	58		T3(15)			31	TCU56	out	res	I6	
	59		T4(0)				TCU63	out	BLK_GRAD_X	A4	
	60		T4(1)				TCU65	out	BLK_GRAD_Y	A5	
	61		T4(2)				TCU64	out	BLK_GRAD_Z	A6	
	62		T4(3)				TCU67	out			
	63		T4(4)				TCU68	out			
	64		T4(5)				TCU69	out			
BP HR MAS							TRIG1	in	Trigger 0	C5	
BSMS SLCB							TRIG2	in	Trigger 1	C6	
TRIG STRAFI							TRIG3	in	Trigger 2	E1	
TRIG Solid MAS							TRIG4	in	Trigger 3	E2	
Ext. Button							EXT_MAN_SUSP	in	Manual Suspend	Z5	
Ext. Button							EXT_MAN_STOP	in	Manual Stop	Z6	
							EX_SGU_RES	in/out	Emergency Stop	Z3	
SGU							SGU_ST	in	STATUS	Z4	
DPP							EXT_GCLK	out	NEXT VALUE	Z1	
							GND				1, 3, 5

Table 2.2: Pin Assignment of the RCP Signals on IPSO 19“ Unit

Boot Operation 2.4

A successful boot operation requires the ethernet connection to the powered TOPSPIN−PC which services a valid “diskless”, the correct BIOS adjustments on the “IPSO Host Controller” and pushing the Power-On button for about 2 seconds.

The successful completion of the boot process can be checked in TOPSPIN by typing:

ha <return>

Or in a LINUX shell by typing:

/opt/topspin/prog/bin/scripts/GetSpectDev −i

Both methods return the IP Address of the connected IPSO.

The boot process is automatically controlled by the DHCP process. Normally there is nothing to configure and thus nothing to set incorrectly. The causes of an unsuccessful boot process can only be:

- LAN Boot in BIOS not enabled. To enable the LAN Boot feature would require the connection of a monitor and a keyboard to the IPSO.
- A corrupted “diskless” on the TOPSPIN−PC, which should be installed again.
- A hardware error, which would necessitate further investigation of the boot process to get some more information.

Investigating the Boot Process 2.4.1

Additional information about the boot process can be obtained from 3 sources and from different phases of the boot sequence

1. By monitoring the POST code display and beep codes (requires no additional resources).
2. By configuring the Hyper Terminal application (Windows) or the “cu” application (LINUX) on theTOPSPIN−PC.(Shows messages of bootloader and LINUX).
3. By connecting a monitor and a keyboard to the IPSO (shows all messages during the boot process and provides access to the BIOS adjustments).

POST Code Display

The Power−on−self−test and configuration routines (POST) start just after Power-on. The POST code points to the individual parts which are currently just running or have stopped in case of an error. This sequence normally ends after about 20 seconds with “C0 = Trying to boot OS”.

The list of references between POST codes and routines may be found in the addendum or can be loaded from the Website of “PHOENIX Technologies Ltd” (Phoenix BIOS 4.0, Rev.6).

The POST code display is undefined after start of Linux.

Table 2.3: Occasionally Occurring BIOS Errors

POST Code	POST Routine	Possible Causes	Recommended Actions
28	Auto size DRAM.	DRAM error.	1.Check insertion of the DRAM in the socket. 2. Exchange DRAM or PC module.
49		Faultily inserted PC−module (host controller).	1. Check insertion of the PC module. 2. Remove the controllers one after the other and try again. 3. Check voltages of the power supply. 4. Exchange the PC−module.
	Unsuccessful PCI configuration.	Any defective Tx− or Rx-controller in the system.	
		Defective RESET sequence.	
60	Check extended memory.	Normal BIOS routine which takes about 10 seconds. The duration depends on the volume of memory.	If the test doesn't finish, check the correct fit of the memory.
98	Search for any extension ROM.	Normal BIOS routine which takes only a few seconds.	If the test doesn't finish, check the correct fit of the PC−module and any PCI connection.
B0	Check for errors, stops at B0 with 2 beeps in case of error.	The timer contains corrupted time and date information.	To recover the content of the timer: 1. Press the RESET button, or, 2. Connect an USB keyboard and press F1 to resume and correct time and date with LINUX, or, 3. Connect a monitor too, press F2 to enter the BIOS setup and correct the time and date or set "Hold on errors" to "NO".
C0	Try to boot.	Successful BIOS process but "No Operating System found".	1.Check Ethernet connection. Yellow LINK LED on? Green Rx/Tx LED active? 2.Check in BIOS if Netboot = yes? (see below) or Netboot is at the top of the list in the submenu "Boot Device Priority" and set the item "Onboard LAN PXL ROM" to "Enabled".

Note: The PC module can be pulled off after removing the 4 screws on top of the Module.

To check or exchange the DRAM, the module has to be opened after removing the 2 screws at its bottom side.

Acoustic Beep Codes

Additional to the POST code display some POST routines sound a beep code on error. This beep code is derived from the hexadecimal POST code of the failing test as follows:

1. The 8−bit error code is broken down to four 2−bit groups.
2. Each group is made one−based (1 through 4) by adding 1.
3. Short beeps are generated for the number in each group.

Example: POST code 16h = 00 01 01 10 = 1−2−2−3 beeps.

The “Hyper Terminal” or “cu” window

The boot messages of the IPSO−OS (LINUX) can be printed in a window of the TOPSPIN−PC. This needs a RS232 connection from tty0 of IPSO to a COM port of the TOPSPIN−PC. For details see the TOPSPIN Installation Guide.

Monitor and Keyboard at IPSO

The most detailed information about the boot process can only be obtained by connecting an additional monitor and a keyboard to the connectors inside of the case. It is then possible to watch the BIOS and Linux messages during the boot sequence and to enter the BIOS setup utility.

Table 2.4: Boot Sequence

	Phase of Boot Sequence	Post Code	POST Beeps	Operation
1.	Power On			
2.	Running POST Code Running POST Code	16h	1−2−2−3	Check BIOS ROM checksum.
		20h	1−3−1−1	Test DRAM refresh.
		22h	1−3−1−3	Test 8742 keyboard controller.
		2Ch	1−3−4−1	RAM failure on address line xxxx*.
		2Eh	1−3−4−3	RAM failure on data bits xxxx* of low byte of memory.
		30h	1−4−1−1	RAM failure on data bits xxxx* of high byte of memory.
		46h	2−1−2−3	Check ROM copyright notice.
		4Ah		
		58h	2−2−3−1	Test for unexpected interrupts.
		59h		
		6Eh		
		87h		
		98h	1−2	Search for option ROMs.
		B0h	1−1	Halt on error.
		C0h		Try to boot.
3.	DHCP Process			IPSO applies for an IP address at the DHCP server.
4.	Running Boot Loader			Load and start of bootloader first message sent to the Hyper Terminal window from boot loader.
5.	Loading the OS			Boot messages of Linux in Hyper Terminal.

Checking the BIOS Setup

This requires a monitor and a keyboard at IPSO.

The majority of BIOS items should retain their default values. The complete list of items and its values can be found in the “Addendum”.

To show the BIOS version press the Pause key after start of booting.

To investigate and modify the BIOS adjustments start the BIOS setup utility by pressing F2 when the following string appears during boot up.

Press <F2> to enter Setup

Selecting incorrect values may cause boot failures. Load setup default values to recover by pressing <F9>.

Table 2.5: BIOS Adjustments

Entry	Meaning	Phoenix BIOS 4.0, Rel. 6.0
Kontron Version		MOD9R111
Network Boot Support?		Yes
Display Control Flat Panel Type		Auto Detect
PNP OS Installed	PCI Bridge Support	no
Onboard LPT	Used for JTAG	enable
Legacy USB Support	Global, Interface 0+1, external	enable
On Chip USB 2 Device	Interface 2+3, intern to Slot A+B	disable
PCI Configuration PCI IRQ Line 1	IRQ select for Line “w”	Auto Select
PCI Configuration PCI IRQ Line 2	IRQ select for Line “x”	Auto Select
PCI Configuration PCI IRQ Line 3	IRQ select for Line “y”	Auto Select
PCI Configuration PCI IRQ Line 4	IRQ select for Line “z”	Auto Select

System Configuration 2.5

System configurations of this context means:

1. During boot the BIOS checks for available hardware on the PCI bus, e.g. inserted controller or PCI cards. It recognizes the bus layout, scans all possible slots (sites) for devices, reads the type of the devices and their required amount of address space, defines and sets the base address of each device, lists all devices found and determines which interrupt line they are connected to.
2. After boot, the AQ driver uses the list of the BIOS, reads some additional registers of some devices and gains the necessary information to decide on which IPSO host model (IPSO 19” Unit or IPSO AQS) the software is coming up.

There is no active role for the user to influence this process other than changing the arrangement of inserted controllers and PCI cards. And normally this should not be necessary. Modifying the arrangement changes the device number of each device and could alter the following situations:

- Which controllers can communicate with each other without having to go over a bridge. This is normally irrelevant.
- Which of the controllers share the same interrupt line with each other and with other devices, e.g. the Ethernet or the tty ports.
- To which priority level of the interrupt controller (there are 15) the interrupt of a device has been routed.

The PCI bus contains 4 interrupt lines (INTw, INTx, INTy, INTz named in BIOS as Line1, Line2,Line3, Line4). The distribution of each controller slot interrupt to one of these lines is hard wired.

Table 2.6: Interrupt Distribution of the IPSO 19“ Unit

	Controller Slot										
	1	2	3	4	5	6	7	8	9	PCI 1	PCI 2
	rctrl	tctrl	fctrl 1	fctrl 2	fctrl 3	fctrl 4	fctrl 5	fctrl 6	fctrl 7		
Line 1	X					X					
Line 2				X	X				X		
Line 3			X					X		X	
Line 4		X					X				X

The decision about routing of Line1/2/3/4 to any of the interrupt priority levels (IRQ) and sharing them with further interrupt sources is made by the BIOS, provided the BIOS parameter “PCI IRQLine” is set to “Auto Select”. These routing‘s can be checked in a LINUX shell with:

cat /proc/interrupts

We do not recommend replacing “Auto Select” with a special IRQ level.

	Highest					Interrupt Priority Order								Lowest
IRQ	0	1	8	9	10	11	12	13	14	15	3	4	5	6	7

Recognition of the Host Model *2.5.1*

Recognition of the host model and the version of the installed controller will be performed by the AQ driver of LINUX in following steps:

1. Search for a PLX device with Sub-device ID = 0x0200 and the IMBF version register implemented.
2. Read the content of the IMBF version register.
3. If IMBF=0xFFFF or 0x0000, > IPSO 19” Unit:

   a. Read the version register SLOT_BRDV on each controller.

   b. SLOT_BRDV=0xXFXX or 0xX0XX > 2MB external RAM on this controller and DSP TMS320C6415

   SLOT_BRDV=0xX1XX > 16MB external RAM on this Controller and DSPTMS320C6415

   SLOT_BRDV=0xX2XX > 128MB external RAM on this Controller and DSP TMS320C6455
4. If IMBF= 0x0001, > IPSO AQS > IPSO AQS HOST including Rx-Controller with 2MB external RAM and DSP TMS320C6415

   a. Read the board version of IPSO AQS ACQ out of the T_BRDV register.

   b. T_BRDV=0x0000 > Tx-controller with 16 MB external RAM and DSPTMS320C6415 on IPSO AQS ACQ.

   c. T_BRDV=0x0200 > Tx-controller with 128 MB external RAM and DSPTMS320C6455 on IPSO AQS ACQ.

Table 2.7: IPSO Versions

IMBF		T_BRDV		SLOT_BRDV			
Variation	Model	Revision	Sub-revision	Slot	Version	Sub-version	
F F F	F	not used					IPSO 19” Unit
0000							
					X F X X		Tx-controller of IPSO 19 Unit Ext RAM 2MB, DSP TMS320C6415
					X 0 X X		
					X 1 X X		Tx-controller of IPSO 19” Unit ext RAM 16MB, DSP TMS320C6415
					X 2 X X		Tx-controller of IPSO 19” Unit ext RAM 128MB, DSP TMS320C6455
0 0 0 1				not used			IPSO AQS HOST, Rx-controller Ext. RAM of 2MB, DSP TMS320C6415
		0 0 0 0					IPSO AQS ACQ, 5 Tx-controller, Ext. RAM 16MB, DSP TMS320C6415
		0 2 0 0					IPSO AQS ACQ, 5 Tx-controller, Ext. RAM 128MB, DSP TMS320C6455

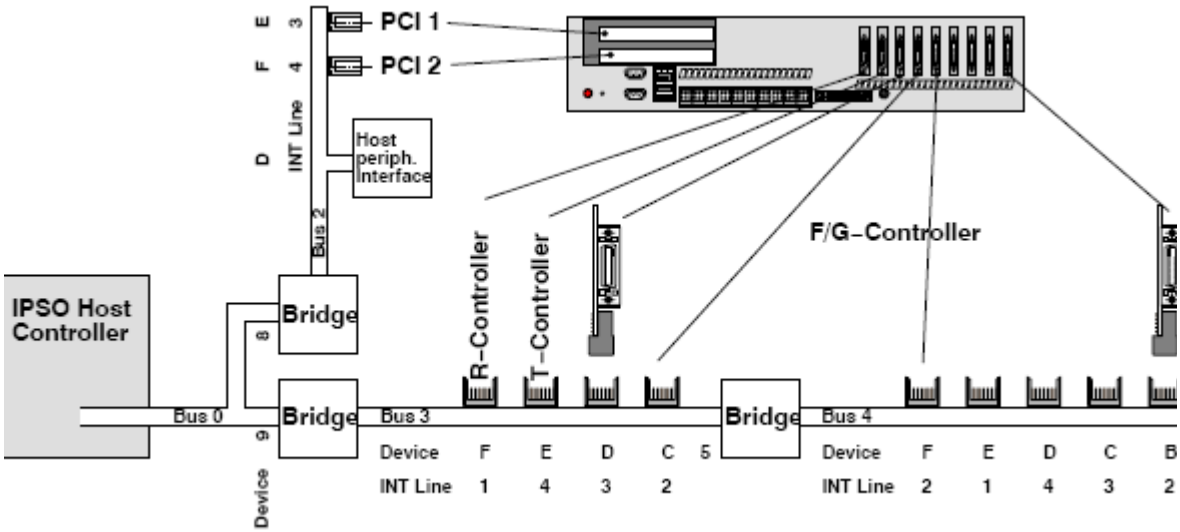


Figure 2.5: Host Bus of the IPSO 19“ Unit

Note: Inserting PCI cards with on−board bridges implies adding further bus segments which can in turn change the bus numbers!

Note: Inserting PCI cards with on−board bridges implies adding further bus segments which can in turn change the bus numbers!

Checking the Configuration 2.5.2

Modification of the system (by inserting or removing controllers or PCI cards) should always be followed by checking the system recognized structure against the expected one. For instance, “has the system accurately recognized the number and the type of all inserted controllers?”.

Starting the IPSOTEST when logged in at the IPSO:

root@IPSO:/opt/test>ipsotest <return>

returns a list of all recognized controllers, their bus and device numbers and their application specific utilization. Bus bridges, general PCI devices and interrupt routing‘s are not shown.

A complete list of all PCI devices and interrupt routing is shown by typing:

root@IPSO:/opt/test>cat /proc/pci <return>

Note: Devices on bus 0 and bus 1 are not application relevant!

Power Supply 2.6

Checking Temperature and Voltages 2.6.1

Typing “mbmon −A” when logged in at the IPSO

root@IPSO:/opt/test>mbmon −A <return>

returns something like the following values provided by voltage and temperature sensors:

Table 2.8: On IPSO 19“ Unit

<table>
<tr><td>Temperature =</td><td>82.0</td><td>80.5</td><td colspan="3">80.5</td><td>So far, these values are not correct.</td></tr>
<tr><td></td><td></td><td></td><td colspan="3">Next to the voltage regulators.</td><td rowspan="3">Sensor location on IPSO Base Board.</td></tr>
<tr><td></td><td></td><td colspan="4">Next to the sequencer.</td></tr>
<tr><td></td><td colspan="5">Below the host controller (PC−module).</td></tr>
<tr><td>Rot. =</td><td>0</td><td>0</td><td>0</td><td></td><td></td><td>Fan speed; not implemented.</td></tr>
</table>

Table 2.8: On IPSO 19“ Unit

Vcore =	1.30	3.41				Core voltage of the host controller.
Voltage =	3.41	5.03	12.46	−11.87	−5.25	Voltages of the power supply.

Note: The -5 Volt from the power supply is not used!

Temperature =	82.0	80.5	80.5			So far, these values are not correct.
			Next to the Rx-controller.			Sensor location on IPSO AQS HOST.
		Next to the PCI connector.				Sensor location on IPSO AQS ACQ.
	Below the host controller (PC−module).					Sensor location on IPSO AQS HOST.
Rot. =	0	0	0			Fan speed; not implemented.
Vcore =	1.30	3.41				Core voltage of the host controller.
Voltage =	3.41	5.03	12.46	−11.87	−5.25	Voltages of the power supply.

Power Conditions on the IPSO 19“ Unit 2.6.2

Table 2.9: Currents and Voltages

Part Number	Assembly		+5 V	Σ +5 V	+3.3 V	+12 V	+5 VSB	-12 V
H12519	IMB	ETX 400 MHz + IMB		2.5 A	2.5 A	0.1	(1.8 A)	0.1
		2 PCI Slot (25 W)		10 A				
		70 RCP/30 mA		2.1 A				
H12538 xx	Tx-controller	1x (0.3 + 0.3)	0.6 A		0	0		0
		8x		4.8 A	0	0		0
H12532 xx	Rx-controller	1x	0.6 A	0.6 A	0	0		0
Current required from ATX power supply				20.0 A	2.5 A	0.1 A	(1.8 A)	0.1 A
Power				108.25 W				
				109.45 W				
				118.15 W				

Power Supply Used *2.6.3*

Any ATX power supply with the same form factor would meet the functional requirements. But to keep the excellent quality and the mark of conformity valid, only the type

eNSP−300P−S20−00S

from the manufacturer Nipron should be used for a replacement.

This installed type is ATX Version 2.03 compliant with 20−pin power connector. Since −5 volts are not required, power supplies with 24−pin connectors (ATX 12V version 2.2) also meet the requirements but need an adapter.

The Nipron power supplies are said to run 24 hours a day during 10 years.

The reliability grade is “Factory Automation” instead of “Office Automation”.

The fan can be replaced without disassembling either the power supply or the IPSO.

Table 2.10: Currents and Voltages

General Specifications			**Continuous Output Specifications**				
			+5 V	**+3.3 V**	**+12 V**	**+5 VSB**	**-12 V**
Part Number	87451		1 A	14 A	10 A	1.5 A	0.8 A
Manufacturer	Nipron		125 W				
Type	eNSP-300P-S20-00S		185 W				
Continuous Power	200 W		203 W				
Peak Power	300 W						
Input	AC85~264 V						
MTBF	100,000 hours						
Safety Standard	UL, CSA (c-UL), EN, CE						

IPSO Organization 3

Table 3.1: Parts and Assemblies for the IPSO 19“ Unit

IPSO CHASSIS UNIT COMPLETE		H9987	
	IPSO 19” RD Case Complete	HZ14023	H1M14023A
	IPSO 19” RD Cover Pane	HZ14022	H4M14022A
	IPSO 19” RD Case Blind	HZ14028	H4M14028C
	Slot sheet for PC−Boards	HZ13609	H2M13609C
	IPSO Ventilator Unit	HZ13594	H3M13594A
	IPSO Mounting Kit	H9986	
	PC Power Supply PC 300W	87451	ENSP−300P−S2 0−00S
	IPSO Base Board	H12519	
	IPSO Base PCB	H12520	H3P2690E
	IPSO Base PCB	H12520F1	H3P2690F
	IPSO Base PCB	H12520F2	H3P2690G
	IPSO Base PCB	H12520F3	H3P2690H
		IPSO ETX Module	H12535	
		PC ETX Module VE−400	86739	
		Heat sink ETX modified	HZ13905	
		SDRAM 512MB SODIMM	87047	
	IPSO TX Board	H12538F2	
	IPSO TX PCB	H12537F4	H4P2760E
	IPSO 19” RD Cover Plate	HZ14029	H4M14029C
	IPSO 19” RD Circuit Lever, large	HZ14030	H2M14030A
	IPSO 19” RD Circuit Lever, short	HZ14031	H2M14031A
	IPSO RX Board	H12532	
	IPSO RX PCB	H12531F1	H3P2770C
	IPSO Display Board	H9975	

Table 3.1: Parts and Assemblies for the IPSO 19“ Unit

	IPSO Display PCB	H9974F1	H4P2790A
	IPSO Display Cable	HZ13591	H4D1391A
IPSO PCI Board		H12524	
	IPSO PCI PCB	H12523F1	H4P2720B
DPP1 Board		H12513F1	
	DPP1 PCB	H12551F3	H4P2820C
PC 2CH RS232 PCI		O10394	EX−41052
PC 4CH RS232 PCI		O10395	EX−41094

LVDS Parts *3.1*

IPSO LVDS Cable		
48−Bit LVDS−Cable, 0,5m, Manufacturer 3M only	88201	14526−EZHB−05 0−0Q
48−Bit LVDS−Cable, 1m, Manufacturer 3M only	86868	14526−EZHB−10 0−0Q
48−Bit LVDS−Cable, 2m, Manufacturer 3M only	87925	14526−EZHB−20 0−0QC
48−Bit LVDS−Cable, 3m, Manufacturer 3M only	87939	14526−EZHB−30 0−0QC
48−Bit LVDS−Cable, 5m, Manufacturer 3M only	87940	14526−EZHB−50 0−0QC

Test Accessories *3.2*

IPSO Test Accessory		
IPSO 19“ trigger test cable	Hz14408	H3D14408A
IPSO CPCI Board	H12521	
IPSO CPCI PCB	H12522	H4P2710

Introduction Status *3.3*

Table 3.2: IPSO 19“ Unit

Part Number	Name	Layout Number	Modification	Program File	Firmware
H12519	IPSO Base Board	H3P2690E	no	IPSO−IMB−2690E00	no
H9975	IPSO Display Board	H4P2790	no	n.a.	no
H12524	IPSO PCI Board				

IPSO Organization

IPSO Host

4

Introduction 4.1

In each IPSO system there is only one IPSO Host comprising of the IPSO Host Controller and its data and control buses and communication interfaces.

The IPSO Host Controller is an IBM compatible PC (ETX−Module) with all standard interfaces. Thus making access possible to the whole pool of standard hardware and software.

Operation 4.1.1

The Host Controller communicates with the TOPSPIN−PC and boots its operating system software (diskless LINUX) from the TOPSPIN−PC via Ethernet. It also communicates over its standard interfaces with the Rx− and the Tx-controllers and with peripheral devices.

Versions

Table 4.1: Host Controller Versions

Location	Name	Part Number	ECL	FW#	Functional Increments	Software Requirements
IPSO 19“	IPSO Base Board	H12519	00			
IPSO 19“	IPSO Base Board	H12519	01		PCI PLX-Int correction.	
IPSO 19“	IPSO Base Board	H12519	02		No, new layout only.	
IPSO 19“	IPSO Base Board	H12519	03		Correction of Flash Prom wiring	
IPSO 19“	IPSO Base Board	H12519	04		No, new layout only.	
IPSO 19“	IPSO Base Board	H12519	05		Due to JTAG programming.	
IPSO 19“	IPSO Base Board	H12519	06		Due to JTAG programming.	
IPSO 19“	IPSO Base Board	H12519	07		3.3 V PCI signal level.	

Features 4.1.2

- ETX Computer Module, up to 512 MByte SDRAM

- 20-pin standard PC ATX Power connector
- 2 PS/2 6 pin header connectors for keyboard and mouse
- 2 PC standard IDE interface and 1 Floppy interface (shared with parallel port)
- Parallel port (shared with floppy)
- Flash Disk Interface (on secondary IDE side)
- 2 PC standard COM/RS232
- 2 USB ports
- VGA output
- 10/100−Mbit Ethernet
- PCI bus with 2 PCI-to-PCI bridge chips able to drive up to 9 devices (IPSO 19” System only)
- PCI bus with 2 PCI-to-PCI bridge chips, driving 6 devices (IPSO AQS System only)
- 2 standard PCI slots, 33MHz, 32 bit, 5V, each system
- Beeper
- Battery for the Real−Time−Clock
- Power On Self Test Decoder
- Temperature/Voltage hardware monitoring
- LED power and control indicators
- JTAG Test/Programing interface
- Coax outputs of the Real-time Control Pulses and Trigger inputs (IPSO 19 inch Unit only)
- BIS Bruker Identification System Flash PROM

Architecture 4.1.3

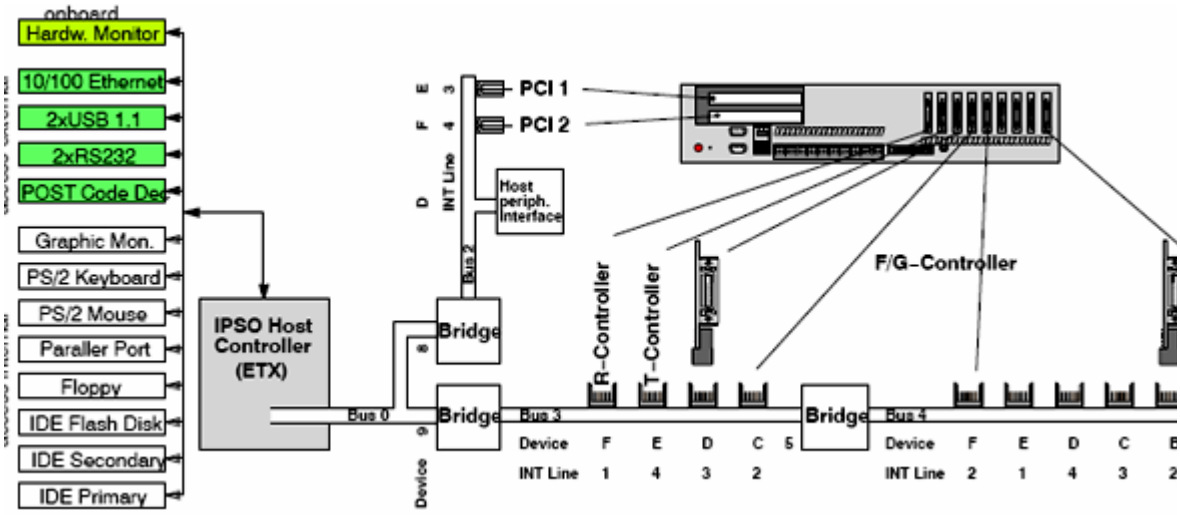


Figure 4.1: IPSO Host of the “IPSO 19 inch Unit”

IPSO Host Controller (ETX−Module) 4.2

The IPSO Host boards are designed to use the Embedded Extended Technology (ETX) modules as Host Controller. All ETX modules feature a stan-

dardized form factor and a standardized connector layout that carry a specified set of signals.

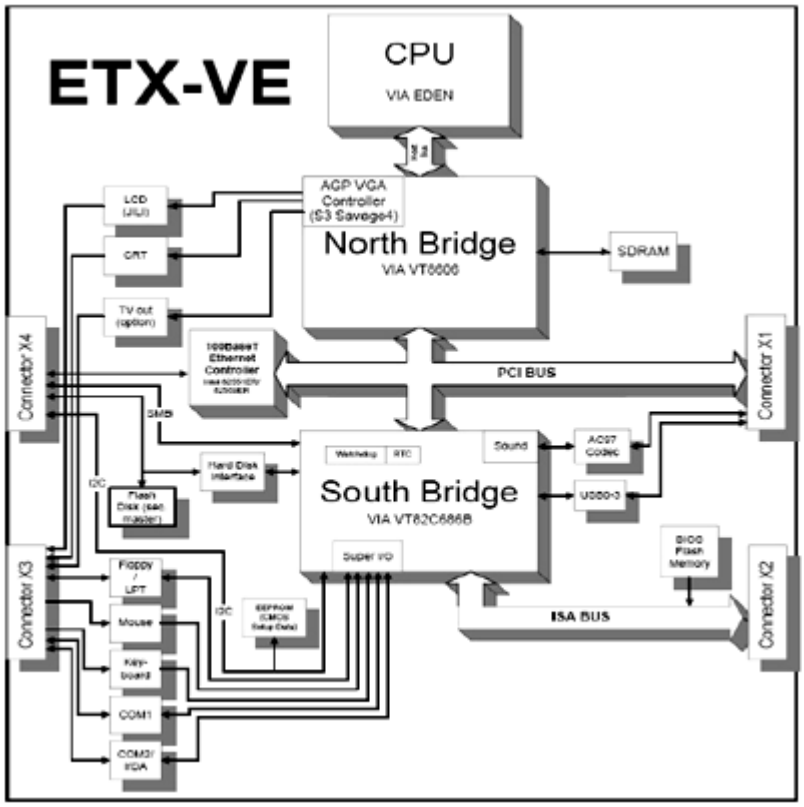


Figure 4.2: Host Controller "ETX VE4" from Kontron

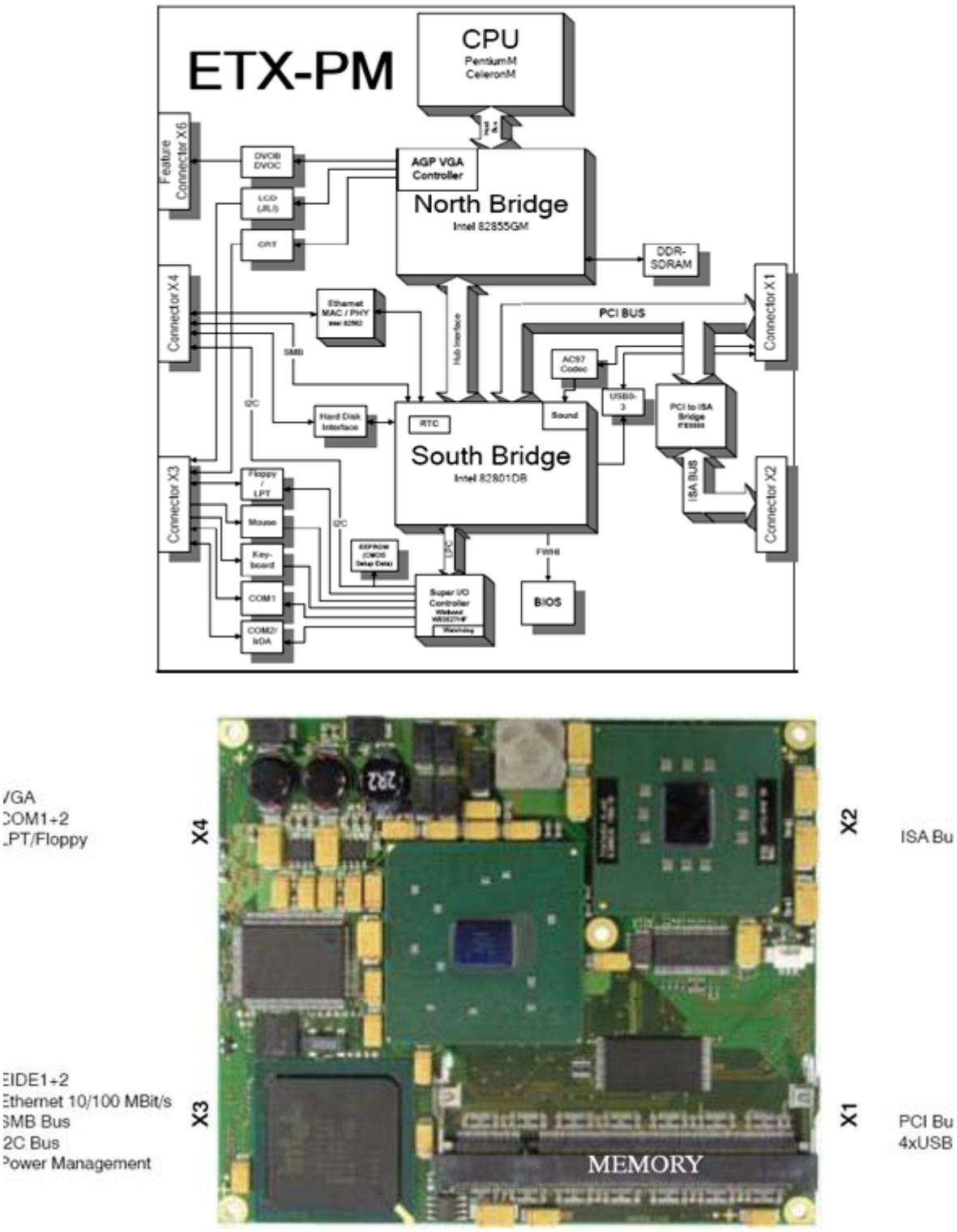


Figure 4.3: Host Controller "ETX PM" from Kontron

Environmental Specifications *4.2.1*

All ETX Modules include a heat spreader plate assembly on the top side. It is NOT a heat sink. The aluminum slugs and thermal pads on the underside of the heat−spreader assembly implement thermal interfaces between the heat spreader plate and the major heat generating components on the ETX module. Under worst case conditions, the cooling mechanism must maintain an ambient air and heat spreader plate temperature of 60° C or less.

Models *4.2.2*

Table 4.2: Selected Types of ETX Modules

	ETX-P1	ETX-VE4	ETX-PM
Revisions	Layout 121, BIOS Rev. 120	Layout 111, BIOS Rev. 110	BIOS Rev. 122
Manufacturer	Kontron	Kontron	Kontron
Component	Intel Platform using Ali Aladdin chip set V M1541, M1543C and Pentium MMX 266MHz processor.	VIA Eden Platform using Twister chip set and ESP4000 400MHz processor.	Intel Celeron M processor 800MHz, L2 cacheless.
CPU Clock	266 MHz	400 MHz	C3 800 MHz
BIOS	Phoenix BIOS 4.0 Release 6.0, Kontron BIOS (MOD5R113) or (MOD9R111).	Phoenix BIOS 4.0 Release 6.0, Kontron BIOS (MOD9R111).	Phoenix BIOS 4.0 Release 6.01 Kontron BIOS (MOD9R122).
DRAM Modules	One SDRAM−SO−DIMM, 144−Pin, 3,3−Volt; 64MB, 128MB, 256MB	One DRAM−SO−DIMM, 144−Pin, 3,3−Volt; 64MB, 128MB, 256MB, 512MB	One DDR−SO−DIMM, 200−Pin, 2,5 Volt; 256MB, 512MB, 1GB
Flash Disk on Module	16MB IDE Flash Disk as IDE2 master devices	None	None
Video Controller	ATI Rage Mobility	Savage S4 (VT8606)	Intel 855GME
Ethernet Controller	Intel 82559ER	Intel 82551ER	Intel 82562
USB Interfaces	0, 1, 2, 3	0, 1, 2, 3	0, 1, 2, 3
5 V Power, Full	2.0 A	1.9 A	2.4 A
5 V Power, Standby	1.4 A	1.4 A	1.28 A
5V Power, Suspend	0.9 A	0.8 A	0.31 A

Layout Dependent Conditions of Choice *4.2.3*

The following attributes are not covered by the ETX Standard. But the have to be defined in PCB layout and logic and therefore must not be ignored in selecting the ETX module.

Table 4.3: IPSO Host, Predefined ETX Requirements

ETX Features which have to meet the Host layout	Necessary at “Bus 0” on IPSO Host
ADxx lines which are supported by the BIOS and ETX for usage on IPSO Host	AD19+AD20
Which REQ/GRANT pairs must be unused on the module and free to be used by the IPSO Host REQ/GRANT_0 REQ/GRANT_1	REQ/GRANT_0 REQ/GRANT_1

BIOS *4.2.4*

The module is equipped with a Phoenix BIOS, which is located in an on-board Flash EEPROM. The device has 8 bit access. Faster access (16 bit) is provided by the shadow RAM. All IPSO host controllers are diskless and require some special BIOS settings:

- Remote Program Load ROM of onboard LAN Controller = Enabled, and,
- LAN boot priority of OS = At first position!

Table 4.4: BIOS Adjustments

Entry	Meaning	Phoenix BIOS 4.0 Release 6.0	Phoenix BIOS 4.0 Release 6.1
Kontron−Version		MOD9R11	MODRB122
Network boot support?		Yes	Yes
Display Control: Flat Panel Type		Auto Detect	Auto Detect
PNP OS Installed	PCI Bridge Support	No	No
Onboard LPT		Enabled	Enabled
Legacy USB Support	Global interface 0 + 1, external.	Enabled	Enabled
On Chip USB 2 Device	Interface 2+3, internal to slot A + B.	Disabled	Disabled
PCI Configuration PCI IRQ Line 1	IRQ select for line „w“	Auto Select	Auto Select
PCI Configuration PCI IRQ Line 2	IRQ select for line „x“	Auto Select	Auto Select

Table 4.4: BIOS Adjustments

Entry	Meaning	Phoenix BIOS 4.0 Release 6.0	Phoenix BIOS 4.0 Release 6.1
PCI Configuration PCI IRQ Line 3	IRQ select for line „y“	Auto Select	Auto Select
PCI Configuration PCI IRQ Line 4	IRQ select for line „z“	Auto Select	Auto Select

For more BIOS settings refer to the Appendix or the Kontron ’’ETX−VE User’s Guide, Document Revision 2.0“ at www.kontron.com. The BIOS can be updated or restored by using a special procedure in factory only.

PCI Bus 4.3

Features 4.3.1

- Conforms to PCI specification revision 2.1.
- 32 bit, 33 MHz.
- Voltage range of signals is (0...5)V or (0...3,3)V dependent on bus number and configuration. Details below.
- Bus [00], [01] are used on ETX module.
- Bus [00] is continued off the module to IPSO Host without using a bridge on the module.

Structure of IPSO 19” Unit Table 4.3.2

Table 4.5: Voltage Level of Signals in Several Bus Segments

Designed Levels of Bus System (V)					Necessary Levels of Devices (V)			
Bus Segment	Layout	Max. Send	Tolerance	Require ment	Device	Tolerance	Require ment	Must Send
Bus [00]	H3P269 0E/ F/G	5	5	3.3	VE4	5	5	3.3
	H3P269 0H	3.3	5	3.3	PM	3.3	3.3	3.3
Bus [02]	All	5	5	3.3	RS232	5	3.3/5	3.3
Bus [03]		3.3	5	3.3	Rx/ TxCtrl	3.3	3.3	3.3
Bus [04]		3.3	5	3.3	TxCtrl	3.3	3.3	3.3

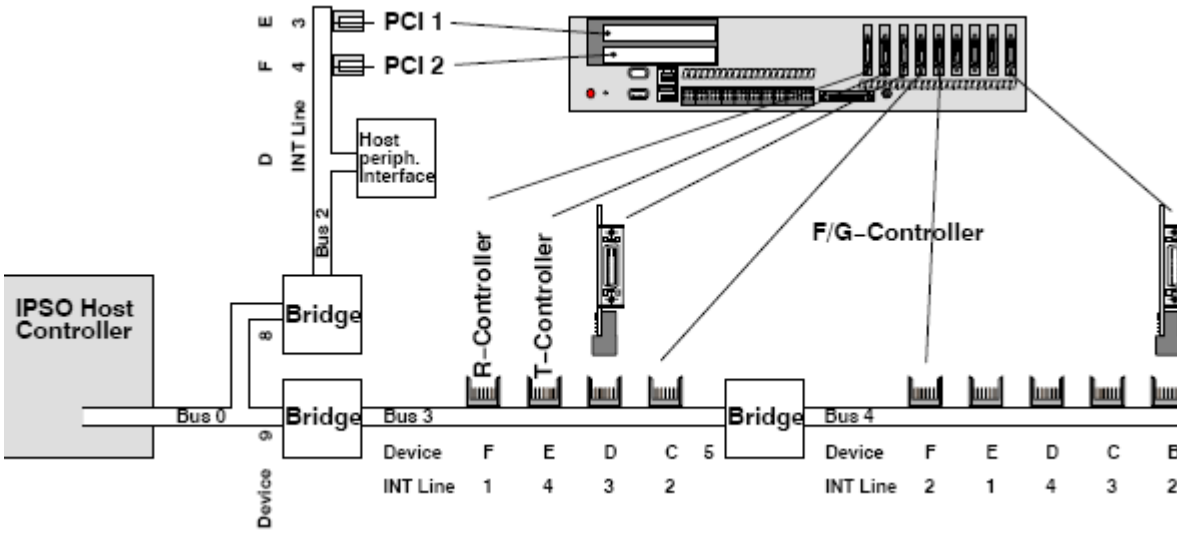


Figure 4.4: Host bus of the IPSO 19" Unit

- At bus [02]: The host peripheral Interface (PLX, dev. 0d.0) and two standard PCI slots as devices 0e.0, 0f.0
- At bus [03]: The PCI/PCI bridge as device 05.0 and 4 Tx/Rx PCI slots as de-vices 0c.0, 0d.0, 0e.0, 0f.0
- At bus [04]: 5 Tx PCI slots as devices 0b.0, 0c.0, 0d.0, 0e.0, 0f.0.

The LINUX command lspci −t prints the following tree picture of that structure:

```
-[00]-+-00.0
      +-01.0-[01]----00.0
      +-02.0
      +-07.0
      +-07.1
      +-07.2
      +-07.4
      +-07.5
      +-08.0-[02]----0d.0
      \-09.0-[03-04]--+-05.0-[04]--
```

Comment: [00] is a PCI Bus name
00.0 is a PCI Device name

Note: Inserting PCI cards with onboard bridges implies adding further bus segments which can in turn change the bus numbers!

Device Dependent Allocation of Signals 4.3.3

Table 4.6: PCI Device Allocation of Special Signals in the IPSO 19" Unit

Bus	Device	Slot	Pin to Signal			
			IDSEL	CLK	INTA at line	REQ/GNT#
0	8	Slot 1 of ETX Bridge: Bus 2	AD19	PCICLK1	-	0
	9	Slot 2 of ETX Bridge: Bus 3	AD20	PCICLK2	-	1
2	D	Host Peripheral Interface (PLX)	B_AD29	B_CLK2	x	Slave device only
	E	Standard Slot PCI1	B_AD30	B_CLK0	y	B_REQ/B_GNT0
	F	Standard Slot PCI2	B_AD31	B_CLK1	z	B-RQ/B_GNT1
3	5	Bridge: Bus 4	S_AD21	S_CLK4	-	REQ/GNT2
	F	rcon R	S_AD31	S_CLK0	w	S_REQ/S_GNT0
	E	tcon A	S_AD30	S_CLK1	z	S_REQ/S_GNT1
	D	con B	S_AD29	S_CLK2	y	S_REQ/GNT2
	C	con C	S_AD28	S_CLK3	x	S_REQ/GNT3
4	F	con D	A_AD31	A_CLK0	x	A_REQ/A_GNT0
	E	con E	A_AD30	A_CLK1	w	A_REQ/A_GNT1
	D	con F	A_AD29	A_CLK2	z	A_REQ/A_GNT2
	C	con G	A_AD28	A_CLK3	y	A_REQ/A_GNT3
	B	con H	A_AD27	A_CLK4	x	A_REQ/A_GNT4

PCI Bus Signals 4.3.4

Standard PCI Connector

The signal assignment to most of the connector pins is fixed as in the following table by the "PCI Local Bus Specification". The assignment to some pins depends on the device address behind of that connector or the signal level environment. They are marked as follows:

Green pins: The device address (INTi, IDSEL) or the request priority (REQ,GNT) dictate the assigned signal.

Blue: The level of the signal voltage (5 or 3.3 Volt) requires that voltage at all of these pins.

Red: All of these pins are reserved for future use. They must not be used at connectors for standard PCI cards.

Table 4.7: Signals at the Standard PCI Connector, 32 bit, 5 or 3.3 Volt

PCI Standard Connector 5V / 3.3V Environment							
Pin	**Row B**	**Pin**	**Row A**	**Pin**	**Row B**	**Pin**	**Row A**
1	-12 V	1	TRST	32	AD17	32	AD16
2	TCK	2	12 V	33	CBE2#	33	3.3 V
3	GND	3	TMS	34	GND	34	FRAME#
4	TDO	4	TDI	35	IRDY#	35	GND
5	VCC	5	VCC	36	3.3 V	36	TRDY#
6	VCC	6	INTA#	37	DEVSEL#	37	GND
7	INTB#	7	INTC#	38	GND	38	STOP#
8	INTD#	8	VCC	39	LOCK#	39	3.3 V
9	PRSNT1	9	res	40	PERR#	40	SDONE
10	res	10	IO-5/3 V	41	3.3 V	41	SB0#
11	PRSNT2	11	res	42	SERR#	42	GND
12	DND	12	GND	43	3.3 V	43	PAR
13	DND	13	GND	44	CBE1#	44	AD15
14	res	14	res	45	AD14	45	3.3 V
15	DND	15	PCIRST#	46	DND	46	AD13
16	PCICLK	16	IO-5/3 V	47	AD12	47	AD11
17	DND	17	GNT#	48	AD10	48	GND
18	REQ#	18	GND	49	GND	49	AD9
19	IO-5/3 V	19	res	50	free	50	free
20	AD31	20	AD30	51	free	51	free
21	AD29	21	3.3 V	52	AD8	52	CBE0#
22	GND	22	AD28	53	AD7	53	3.3 V
23	AD27	23	AD26	54	3.3 V	54	AD6
24	AD25	24	AD24	55	AD3	55	AD4
25	3.3 V	25	AD24	56	AD3	56	GND
26	CBE3#	26	IDSEL	57	GND	57	AD2

Table 4.7: Signals at the Standard PCI Connector, 32 bit, 5 or 3.3 Volt

PCI Standard Connector 5V / 3.3V Environment								
Pin	**Row B**	**Pin**	**Row A**		**Pin**	**Row B**	**Pin**	**Row A**
27	AD23	27	3.3 V		58	AD1	58	AD0
28	GND	28	AD22		59	IO-573 V	59	IO-573 V
29	AD21	29	AD20		60	ACK64= PULLUP0	60	REQ64= PULLUP1
30	AD19	30	AD20		61	VCC	61	VCC
31	3.3 V	31	AD18		62	VCC	62	VCC

Rx/Tx−Connectors at Bus3 and 4; IPSO−Rx and IPSO−Tx

There are 9 CPCI slots of it 4 at the bus [03] and 5 at the bus [04]. The signal assignment to most of the Compact PCI connector pins is fixed as in the following table and very nearly to “CPCI Local Bus Specification”. For details slot interrupt routing show Table: INTA wiring on PC−Module “ETX−P1” and IPSO Host of the IPSO 19inch Unit.

Table 4.8: Pin Destinations of Signals at the Reserved Pins of ST10−ST13

Different Destination at Bus [03] of ST10...ST13 Connectors					
Pin	**Row A**	**Row B**	**Row C**	**Row D**	**Row E**
1	+5.0 V		TRSTB_A*	USBPWR_R/A-C	+5.0 V
2	TCKB_A	+5.0 V	TMSB_A	TDOB	TDIB_A
3	INTA_R/A-C*	INTB_R/A-C*	INTC_R/A-C*	+5.0 V	INTD_R/A-C*
4	+2.5 V	GND	+3.3 V	+1.4V_D	+1.4V_D
5	+2.5 V	BRSVP1B5	S_RST*	GND	S_GN0-3*
6	S_REQ0-3*	GND	+3.3 V	S_CLK0-3	S_AD31
7	S_AD30	S_AD29	S_AD28	GND	S_AD27
8	S_AD26	GND	+3.3 V	S_AD25	S_AD24
9	S_CBE3*	S_IDSEL_R/A-C*	S_AD23	GND	S_AD22
10	S_AD21	GND	+3.3 V	S_AD20	S_AD19
11	S_AD18	S_AD17	S_AD16	GND	S_CBE2*
12	+3.3 V	S_FRAME*	S_IRDY*	GND	S_TRDY*
15	+3.3 V	S_FRAME*	S_IRDY*	GND	S_TRDY*

Table 4.8: Pin Destinations of Signals at the Reserved Pins of ST10−ST13

Different Destination at Bus [03] of ST10...ST13 Connectors					
Pin	**Row A**	**Row B**	**Row C**	**Row D**	**Row E**
16	S_DEVSEL*	GND	+3.3 V	S_STOP*	S_LOCK*
17	+3.3 V	S_SDONE*	S_SBO*	GND	S_PERR*
18	S_SERR*	GND	+3.3 V	S_PAR*	S_CBE1*
19	+3.3 V	S_AD15	S_AD14	GND	S_AD13
20	S_AD12	GND	+3.3 V	S_AD11	S_AD10
21	+3.3 V	S_AD9	S_AD8	S_M66EN	S_CBE0*
22	S_AD7	GND	+3.3 V	S_AD6	S_AD5
23	+3.3 V	S_AD4	S_AD3	+5.0 V	S_AD2
24	S_AD1	+5.0 V	+3.3 V	S_AD0	S_ACK64*
25	+5.0 V	+USB_R/A-C	-USB_R/A-C	+3.3 V	+5.0 V

Table 4.9: Pin Destinations of Signals at the Reserved Pins of ST14-ST18

Different Destination at Bus [04] of ST14...ST18 Connectors					
Pin	**Row A**	**Row B**	**Row C**	**Row D**	**Row E**
1	+5.0 V		TRSTB_B*	USBPWR_D-H	+5.0 V
2	TCKB_B	+5.0 V	TMSB_B	TDOB	TDIB_B
3	INTA_D-H*	INTB_D-H*	INTC_D-H*	+5.0 V	INTD_D-H*
4	+2.5 V	GND	+3.3 V	+1.4V_D	+1.4V_D
5	+2.5 V	BRSVP1B5	A_RST*	GND	A_GN0-4*
6	A_REQ0-4*	GND	+3.3 V	A_CLK0-4	A_AD31
7	A_AD30	A_AD29	A_AD28	GND	A_AD27
8	A_AD26	GND	+3.3 V	A_AD25	A_AD24
9	A_CBE3*	A_IDSEL_D-H*	A_AD23	GND	A_AD22
10	A_AD21	GND	+3.3 V	A_AD20	A_AD19
11	A_AD18	A_AD17	A_AD16	GND	A_CBE2*
15	+3.3 V	A_FRAME*	A_IRDY*	GND	A_TRDY*
16	A_DEVSEL*	GND	+3.3 V	A_STOP*	A_LOCK*
17	+3.3 V	A_SDONE*	A_SBO*	GND	A_PERR*

Table 4.9: Pin Destinations of Signals at the Reserved Pins of ST14-ST18

Different Destination at Bus [04] of ST14...ST18 Connectors					
Pin	**Row A**	**Row B**	**Row C**	**Row D**	**Row E**
18	A_SERR*	GND	+3.3 V	A_PAR*	A_CBE1*
19	+3.3 V	A_AD15	A_AD14	GND	A_AD13
20	A_AD12	GND	+3.3 V	A_AD11	A_AD10
21	+3.3 V	A_AD9	A_AD8	A_M66EN	A_CBE0*
22	A_AD7	GND	+3.3 V	A_AD6	A_AD5
23	+3.3 V	A_AD4	A_AD3	+5.0 V	A_AD2
24	A_AD1	+5.0 V	+3.3 V	A_AD0	A_ACK64*
25	+5.0 V	+USB_D-H	-USB_D-H	+3.3 V	+5.0 V

Adapting the Standard Slots “PCI 1” and “PCI 2” to PCI Bus “2” 4.3.5

IPSO 19inch Unit

The IPSO PCI Board (H12524) is attached via the PCI bus connector ST44. Due to the fact that its reserved pins had to been used for the additional signals dedicated to the standard slots PCI1 and PCI2, ST44 is not qualified for insertion of any Standard PCI Card.

ST44 is dedicated for the insertion of H12524 only!

The following table shows only the anomalous signal wiring between ST44 and PCI1 respective PCI2:

Table 4.10: Pin Destinations of Signals at the Reserved Pins of ST44

ST44		Different Destination at	
Pin	**Row B**	**PCI 1**	**PCI 2**
1	-12V		
2	TCK		
3	GND		
4	TDO		
5	VCC		
6	VCC		

ST44		Different Destination at	
Pin	**Row A**	**PCI 1**	**PCI 2**
1	TRST		
2	12 V		
3	TMS		
4	TDI		
5	VCC		
6	y	A6	B8

Table 4.10: Pin Destinations of Signals at the Reserved Pins of ST44

ST44		Different Destination at			ST44		Different Destination at	
Pin	Row B	PCI 1	PCI 2		Pin	Row A	PCI 1	PCI 2
7	z	B7	A6		7	w	A7	B7
8	x	B8	A7		8	VCC		
9	PRSNT1				9	TDO	B4	B4
10	REQ1		B18		10	IO-5/3 V		
11	PRSNT2				11	res		
12	GND				12	GND		
13	GND				13	GND		
14	CLK1		B16		14	GNT1		A17
15	GND				15	PCIRST#		
16	CLK0	B16			16	IO-5/3 V		
17	GND				17	GNT0	A17	
18	REQ0	B18			18	GND		
19	IO-5/3 V				19	res		
20	AD31				20	AD30		
21	AD29				21	3.3 V		
22	GND				22	AD28		
23	AD27				23	AD26		
24	AD25				24	GND		
25	3.3 V				25	AD24		
26	CBE3#				26	IDSEL		
27	AD23				27	3.3 V		
28	GND				28	AD22		
29	AD21				29	AD20		
30	AD19				30	GND		
31	3.3 V				31	AD18		

All other pins are connected at PCI1 and 2 to the same destination pin as at ST44.

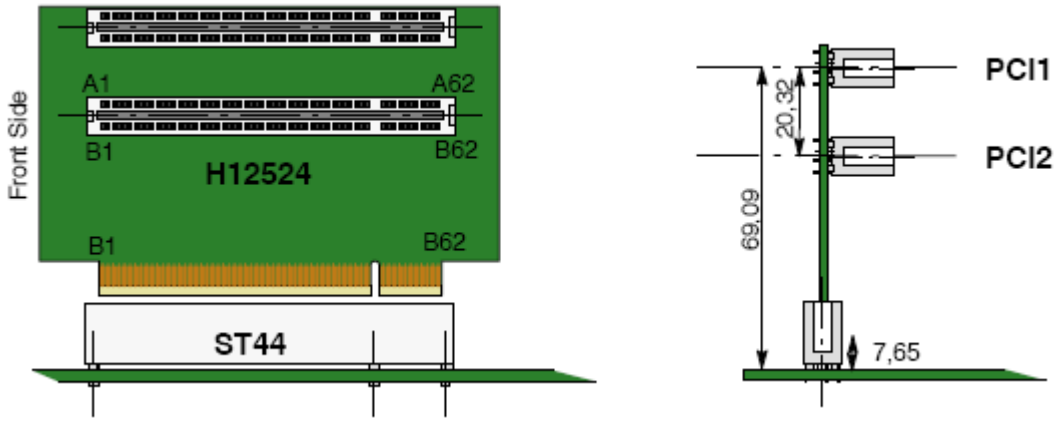


Figure 4.5: Adapter IPSO PCI Board, H12524.

PCI Devices *4.3.6*

Outside the ETX−Module, there are only two different PCI interface devices which are used numerously:

- The DSP TMS320C6415 with PCI interface from TI
- The PCI target controller “PCI9030” from “PLX Technology” as Host Peripheral Interface.

The PCI Interface of DSP “C6415”

Address Mapping

Table 4.11: Access Ranges for the DSP C6415

External Bus Access				To DSP Internal			
Space	**Access Type**	**Address**		**Address**	**Range**	**Destination**	
Memory	Prefetchable Memory	Bit [31...22]	<Base0>	<DSPP>	The whole memory range is accessible through this 4 Mbyte Window		
		Bit [21...0]	AD [21..0]		64 MB	0x600-63F	EMIFB 0
					64 MB	0x640-67F	EMIFB 1
					64 MB	0x680-6BF	EMIFB 2
					64 MB	0x6C0-6FF	EMIFB 3
					256 MB	0x800-8FF	EMIFA 0 :MEM
					256 MB	0x900-9FF	EMIFA 1 :FIFO
					256 MB	0xA00-AFF	EMIFA 2
					256 MB	0xB00-BFF	EMIFA 3
8 MB Reg. Memory	Single Access Non-prefetchable Register	Bit [31...23]	<Base1>	[0000 0001 1]$_2$	Fixed 8 MB Register Window: 0x0180... 0x01FF		
						0x01C00000	11 Register
		Bit [22...03]	AD [22...0]			0x01C20000	3 Register
						0x01C1FFF0	HSR reg.
						0x01C1FFF4	HDCR reg.
						0x01C1FFF8	DSPP reg.
I/O	Single Access Non-prefetchable Register	Bit [31...4]	<Base2>		I/O Space		HSR HDCR DSPP
		Bit [3...0]	AD [3...0]				

The Host Peripheral Interface (HPI) *4.3.7*

The Host Peripheral Interface uses the PCI Target bridge PLX 9030. This device connects the local bus of the “Host Peripheral Interface” to the PCI bus and supports read and write accesses from PCI to local bus.

The Local Bus of the HPI is connected to following devices:

- IPSO Configuration Register, containing hardware information
- FLASH PROM, containing BIS information (BIS = Bruker Information System)
- JTAG Interface, making the JTAG chain accessible to the software and allowing reprogramming of the hardware logic by the system itself.

Furthermore to the HPI, the PLX 9030 is used at the PCI Bus of IPSO on the PCI Standard Devices “IPSO DPP1” and “IPSO DPP2”. The configuration space of these 3 devices can be recognized by the different content of their “Subsystem ID Registers”. The different configuration spaces of the PLX 9030 are stored in 4−Kbyte Serial EEPROMs of type “93CS66L”. These PROMs are read by the PLX 9030 when the PCI reset is deasserted. The PROM contents can be created using the “PLXMon” software and stored using the JTAG Tool of GOEBEL.

The contents of the PCI configuration space registers can be checked in the print out of the command lspci −x, typed in a LINUX shell.

Table 4.12: Configuration Space of the Host Peripheral Interface, PLX

Hex Addr. „xy“	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0y	b5	10	30	90	03	01	90	02	0a	00	80	06	08	00	00	00
1y	00	00	26	e8	01	90	00	00	00	00	30	e8	00	00	22	e8
2y	00	00	21	e8	00	00	20	e8	00	00	00	00	00	00	00	02
3y	00	00	00	00	40	00	00	00	00	00	00	00	0a	01	00	00

Table 4.13: Meaning and 4byte Data of the HPI Configuration Space

HPI PCI Configuration Registers					
Offset	**Register**	**Value**	**Offset**	**Register**	**Value**
0x00	Dev/Vendor ID	0x903010b5	0x3c	Int. Pin Line	0x000001f
0x04	PCI/Cmd Status	0x00100000	0x40	PM Capabilities	0x48014801
0x08	Class Code/Rev.	0x0680000a	0x44	PM Cntrl/Status	0x00000000

Table 4.13: Meaning and 4byte Data of the HPI Configuration Space

HPI PCI Configuration Registers					
Offset	**Register**	**Value**	**Offset**	**Register**	**Value**
0x2c	Subsystem ID/ Subvendor ID	0x02000000	0x48	HS Cntrl/NCP	0x00004c06
0x34	New Cap Pointer	0x00000040	0x4c	VPD Cntrl/NCP	0x00000003

The 16−bit Subsystem ID is stored at addresses 0x2F and 0x2E. The Subsystem ID for IPSO PCI devices using the PLX 9030 is:

Table 4.14: PLX Subsystem ID of IPSO Devices

	IPSO DPP1	**IPSO DPP2**	**IPSO Host Port Interface**
PLX Subsystem ID	0x0100	0x0101	0x0200

This is default PLX EEPROM register set (IMB00AB05.dat) after power−on condition.

Table 4.15: IPSO19"/AQS PLX Memory Space Register

PLX Memory Space0 Registers		
Offset	**Register**	**Value**
0x28	Descriptor	0x00400002
0x00	Range	0x00ff00000
0x14	Remap	0x00000001

PLX Memory Space1 Registers		
Offset	**Register**	**Value**
0x2c	Descriptor	0x50400040
0x04	Range	0x00ff00000
0x18	Remap	0x00000001

PLX Memory Space2 Registers		
Offset	**Register**	**Value**
0x30	Descriptor	0x50400040
0x08	Range	0x00ff00000

Table 4.15: IPSO19”/AQS PLX Memory Space Register

0x1c	Remap	0x00000001

PLX Memory Space3 Registers		
Offset	**Register**	**Value**
0x34	Descriptor	0x50400040
0x0c	Range	0x00ff00000
0x20	Remap	0x00000001

Table 4.16: IPSO19”/AQS PLX Chip Select Register

PLX Chip Select Registers		
Offset	**Register**	**Value**
0x3c	CS0 Base	0x00000000
0x40	CS1 Base	0x00000000
0x44	CS2 Base	0x00000000
0x48	CS3 Base	0x00000000

Table 4.17: IPSO19”/AQS PLX Control Register

PLX Control Registers		
Offset	**Register**	**Value**
0x4c	Int Cntrl/St	0x00300040
0x50	Eep/trgt Ctrl	0x00780000
0x54	GP I/O	0x00249000
0x70	PM Select	0x00000000
0x74	PM Scale	0x00000000

Table 4.18: IPSO19”/AQS PLX Expansion ROM Register

PLX Expansion ROM Registers		
Offset	**Register**	**Value**

Table 4.18: IPSO19"/AQS PLX Expansion ROM Register

0x38	Descriptor	0x00000000
0x10	Range	0x000000000
0x24	Remap	0x00010000

Hardware Configuration Register *4.3.8*

The Configuration Register indicates configuration of IPSO boards. It is a fix wired 16 Bit register mapped in Space 0 of the PLX9030.

Table 4.19: IPSO Hardware Configuration Register

IPSO Hardware Configuration Register	
IPSO 19“	b 0000 0000 0000 0000
IPSO AQS	b 0000 0000 0000 0001

Bruker Identification System Flash PROM

The Flash PROM is mapped in Space 3 of the PLX9030 device. It contains following information and can be read with the “IPSO Web Administration Tool”:

- Device type
- Part number
- Serial number
- EC Level
- Name
- Production date
- Firmware version
- Flash write count

Table 4.20: IPSO Flash Signal Description

Signal	Description
Flash_CS*	Flash Chip Select. When asserted low, the flash PROM is forced to enter a read or write cycles.
Flash_WR*	Flash Write Signal. When asserted low, the flash PROM is forced to write access.
Flash_OE*	Flash Output Enable signal. When asserted low, the flash PROM is forced to read access. Is driven low automatically when the PCI9030 owns the local bus.

PLX JTAG Interface *4.3.9*

The JTAG interface is used for the IPSO firmware update and accessible by PLX General Purpose I/O port (for more details show IPSO firmware update manual).

Table 4.21: PLX Gen. Purpose I/O Control and JTAG Interface (GPIO: 54h)

Bit	Description	Read/Write	Value after Reset	Initial Value	Signal Name	I/O
0	GPIO0	Yes	0	0		
1	GPIO0 Direction	Yes	0	1		
2	GPIO0 Data	Yes	0	0		
3	GPIO1	Yes	0	0		Output n/u
4	GPIO1 Direction	Yes	0	1		
5	GPIO1 Data	Yes	0	1/0	TRST*	JTAG Output
6	GPIO2	Yes	0	0		
7	GPIO2 Direction	Yes	0	1		
8	GPIO2 Data	Yes	0	0		Output n/u
9	GPIO3	Yes	0	1		
10	GPIO3 Direction	Yes	0	1		
11	GPIO3 Data	Yes	0	1/0	Flash_CS*	Output
12	GPIO4	Yes	1	0		
13	GPIO4 Direction	Yes	0	1		
14	GPIO4 Data	Yes	0	1/0	Flash_WE*	Output
15	GPIO5	Yes	1	0		
16	GPIO5 Direction	Yes	0	1		
17	GPIO5 Data	Yes	0	1/0	TDI	JTAG Output
18	GPIO6	Yes	1	0		
19	GPIO6 Direction	Yes	0	1		
20	GPIO6 Data	Yes	0	1/0	TMS	JTAG Output
21	GPIO7	Yes	1	0		
22	GPIO7 Direction	Yes	0	1		
23	GPIO7 Data	Yes	0	1/0	TCK	JTAG Output

Table 4.21: PLX Gen. Purpose I/O Control and JTAG Interface (GPIO: 54h)

Bit	Description	Read/Write	Value after Reset	Initial Value	Signal Name	I/O
24	Reserved	Yes	0	0		
25	GPIO8 Direction	Yes	0	0		
26	GPIO8 Data	Yes	0	1/0	TDO	JTAG Input
27-31	Reserved	Yes	0h	0h		

Note: GPIO pins configured as output are driven only when the PCI9030 controls the local bus.

- (*) indicates low active signal
- (1/0) indicates high or low transaction

Table 4.22: JTAG Signal Description

Signal	Description
TRST*	JTAG TAP reset. When asserted low, the TAP controller is asynchronously forced to enter a reset state, which in turn asynchronously initializes other test logic. An non-terminated TRST_I produces the same result as if it were driven high. The TAP controller must be reset before the chip can function in normal operating mode.
TMS	JTAG test mode select. Signal TMS causes state transitions in the test access port (TAP) controller. An non-driven TMS has the same result as if it were driven high.
TCK	JTAG boundary scan clock controlling the JTAG logic.
TDI	JTAG serial data in. Signal TDI is the serial input through which JTAG instructions and test data enter the JTAG interface. The new data on TDI is sampled on the rising edge of TCK. An non-terminated TDI produces the same result as if TDI were driven high.
TD0	JTAG serial data out. Signal TDO is the serial output through which test instructions and data from the test logic.

PCI Interrupt Routing *4.3.10*

The BIOS checks during the configuration phase of the boot process the bus structure and the addresses of the devices found. Based on these results it deduced the interrupt wiring and answered the question, “to which interrupt line of w, x, y or z is a device connected to with its interrupt pin “A” (INTA) (“B”, “C” or “D” if implemented). With this knowledge, the BIOS configures the interrupt router and defines the IRQ level of any device in the system.

Connection of PCI Devices to the INT−Lines *4.3.11*

The following table indicates which PCI interrupt line out of “w, x, y and z” is connected to pin INTA of each PCI device.

Table 4.23: INTA Wiring on “ETX−P1” and IPSO Host of the IPSO−19U

ETX-P1 INT Routing (on module)					**circular INT Routing (on host)**								
INT Line	**Device on Bus 1**		**Device on Bus 0**		**INT Line**	**Device on Bus 0**		**Device on Bus 2**		**Device on Bus 3**		**Device on Bus 4**	
			0	Host Bridge: Bus 0	w			0					
w	0	VGA	1	PCI Bridge: Bus 1	x			1		0			
z	1		2	ETH	y			2		1		0	
w	2		3	Audio	z			3		2		1	
	3		4		w			4		3		2	
	4		5		x			5		4		3	
	5		6		y			6		5	PCI Bridge: Bus 4		
	6		7	ISA Bridge	z			7		6		5	
	7				w	8	Slot 1: PCI Bridge: Bus 2	8		7		6	
	8				x	9	Slot 2: PCI Bridge: Bus 2	9		8		7	
	9				y	A	Slot 3: free	A		9		8	
	A				z	B	Slot 4: free	B		A		9	
	B		C		w			C		B		A	
	C		D		x			D		C	Slot C: FCtrl 2	B	Slot H: FCtrl 7

Table 4.23: INTA Wiring on “ETX−P1” and IPSO Host of the IPSO−19U

ETX-P1 INT Routing (on module)					circular INT Routing (on host)								
INT Line	**Device on Bus 1**		**Device on Bus 0**		**INT Line**	**Device on Bus 0**		**Device on Bus 2**		**Device on Bus 3**		**Device on Bus 4**	
	D		E		y			E	PCI Slot 1	D	Slot B: FCtrl 1	C	Slot G: FCtrl 6
	E		F		z			F	PCI Slot 2	E	Slot A: TCtrl	D	Slot F: FCtrl 5
	F		10	IDE	w					F	Slot R: RCtrl	E	Slot E: FCtrl 4
			11		x							F	Slot D: FCtrl 3
			12		y								
			13		z								
			14		w								

PCI INT−Lines Routing to Prioritized X86−architecture IRQs

Table 4.24: INT Line Assignment

Priority	**PC Cascaded INT Controller**		**ETX On-module Devices**	**Routable, Dependant on BIOS and Equipment**		
				ETX-P1: Phoenix BIOS	**ETX-VE4: Phoenix BIOS**	**ETX-PM: Phoenix BIOS**
Highest	IRQ 0		Timer			

Table 4.24: INT Line Assignment

Priority	PC Cascaded INT Controller		ETX On-module Devices	Routable, Dependant on BIOS and Equipment		
				ETX-P1: Phoenix BIOS	ETX-VE4: Phoenix BIOS	ETX-PM: Phoenix BIOS
	IRQ 1		Keyboard			
	IRQ 2	IRQ 8	RTC			
		IRQ 9	ETH, VGA, USB	PCI INTw: RCtrl, FCtrl 4		
		IRQ 10		PCI INTy: FCtrl 1, FCtrl 6		
		IRQ 11		PCI INTz: TCtrl, FCtrl 5		
		IRQ 12	PS/2 Mouse			
		IRQ 13	FPU			
		IRQ 14	IDE1			
		IRQ 15	IDE2			
	IRQ 3		COM 2			
	IRQ 4		COM 1			
	IRQ 5		Audio	PCI INTx: FCtrl 2, FCtrl 3, FCtrl 7		
	IRQ 6		Floppy			
Lowest	IRQ 7		Parallel Port			

System Management Bus (SMB) *4.4*

The System Management Bus (SM-Bus) is a two wire interface through which various system component chips can communicate with each other and with the rest of the system. It is based on the principles of operation of I2C*.

Function *4.4.1*

The Winbond IC W83782D simultaneously monitor following temperatures and voltages:

- Temperature of ETX Module

- Temperature between Power regulators (IPSO 19” Host only)
- Temperature of Stratix (IPSO 19” Host only)
- Temperature of ACQ DSPs (IPSO AQS Host only)
- 3.3V, 5.0V, 5V_SB,−5V,−12V,12V,VBat

Devices *4.4.2*

Each device that uses the System Management Bus (SMB) has a unique address called the *Slave Address.*

The following slave addresses are reserved by I2C specification and thus cannot be used by any devices of the devices on this particular interface:

Table 4.25: SMB Device Identification - Slave Address

Slave Address Bits 7-1	R/W Bit - Bit 0	Description
0000 000	0	General call address.
0000 000	1	Start byte.
0000 001	X	CBUS address.
0000 010	X	Address reserved for different bus format.
0000 011	X	Reserved for future use.
0000 1XX	X	Reserved for future use.
1111 0XX	X	10 bit slave addressing.
1111 1XX	X	Reserved for future use.

In addition the following address are reserved for the system management bus:

Table 4.26: SMB Reserved Slave Address

Slave Address	Description
0001 000	SMB host.
0001 100	SMB alert response address.
1100 001	SMB device default address.
0101 000	Reserved for access bus host.

Table 4.26: SMB Reserved Slave Address

Slave Address	Description
0110 111	Address reserved for different bus format.
1001 1XX	Unrestricted address.

Table 4.27: ETX−VE Reserved SMB Slave Address

Slave Address Bits 7-1	SMB Device	Description
0001 001	SMART_CHANGER	Not to be used with any SMB device except a changer.
0001 010	SMART_SELECTOR	Not to be used with any SMB device except a selector.
0001 011	SMART_BATTERY	Not to be used with any SMB device except a battery.
1001 110	Temperature Sensor (LM84)	Onboard temperature sensor. Do not connect off board.
1010 000	SPD	SDRAM EEPROM.
1101 001	Clock Generator	Do not use under any circumstances.
0101 101	Reserved	Do not use.

Table 4.28: IPSO Reserved SMB Slave Address

Slave Address Bits 7-0	SMB Device	Description
00101 010	IPSO WINBOND	Temperature/Voltage Control.

Table 4.29: IPSO Winbond SMB First Serial Slave Address

Slave Address 7-3	Bit 2/Pin 45	Bit 1/Pin 46	Bit 0/Pin 47
00101	0	1	0

Note: The Winbond IC W83782D Pin 43 must be set to high.

Reset and Power−ON *4.5*

There are 3 sources of reset functions with different effects:

- The Power−ON/OFF button
- The Reset button
- The Warm−Reset−Bit in the HSR register

Reset Logic *4.5.1*

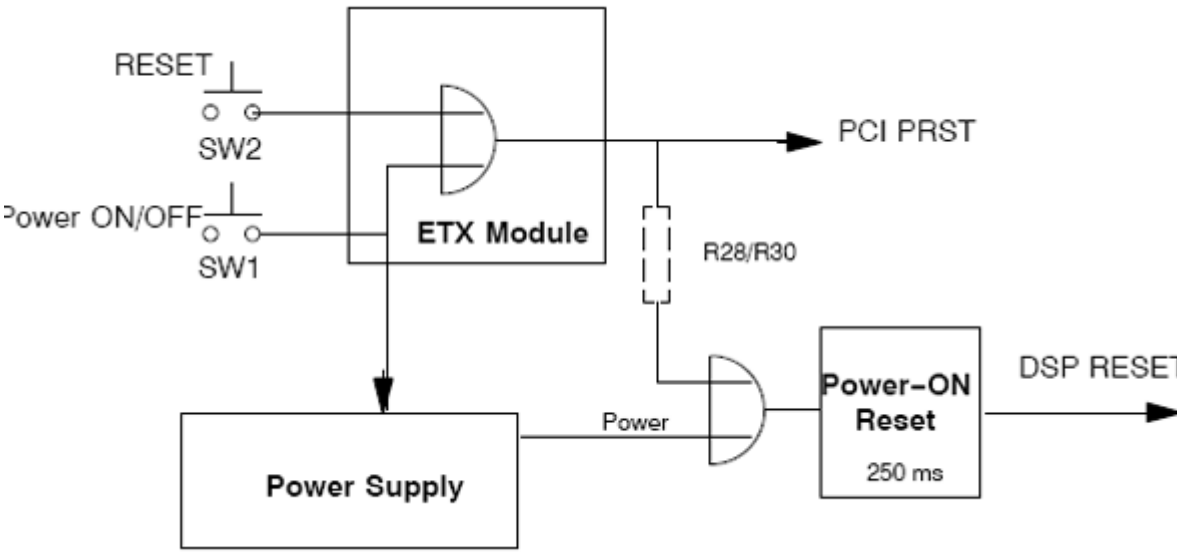


Figure 4.6: Effect of Reset Buttons

Table 4.30: Reset Functions

RESET Sources		**DSP RESET Controls**	
	WARM RESET	**DSP pin $\overline{\text{RESET}}$=0**	**PCI $\overline{\text{PRST}}$=0**
SW1: Power ON/OFF		x	x
SW2: Reset			x
DSP PCI IO Reg HDCR	x		
Controlled Functions			
Reset of PC−Module		x	x
Sample of DSP Config Pins		x	
DSP ConfigReg Reset			x
DSP ConfigReg read from EEPROM			x
Reset of DSP PCI IO−Reg		Bit number dependant	

Table 4.30: Reset Functions

Reset of DSP Memory mapped Reg	x	x	Bit number dependant
DSP PCI FIFO Reset	(x)?		x
DSP Core Reset	x		
DSP Peripheral Logic Reset	x		
DSP awaking from power down modes	x		

Reset Timing *4.5.2*

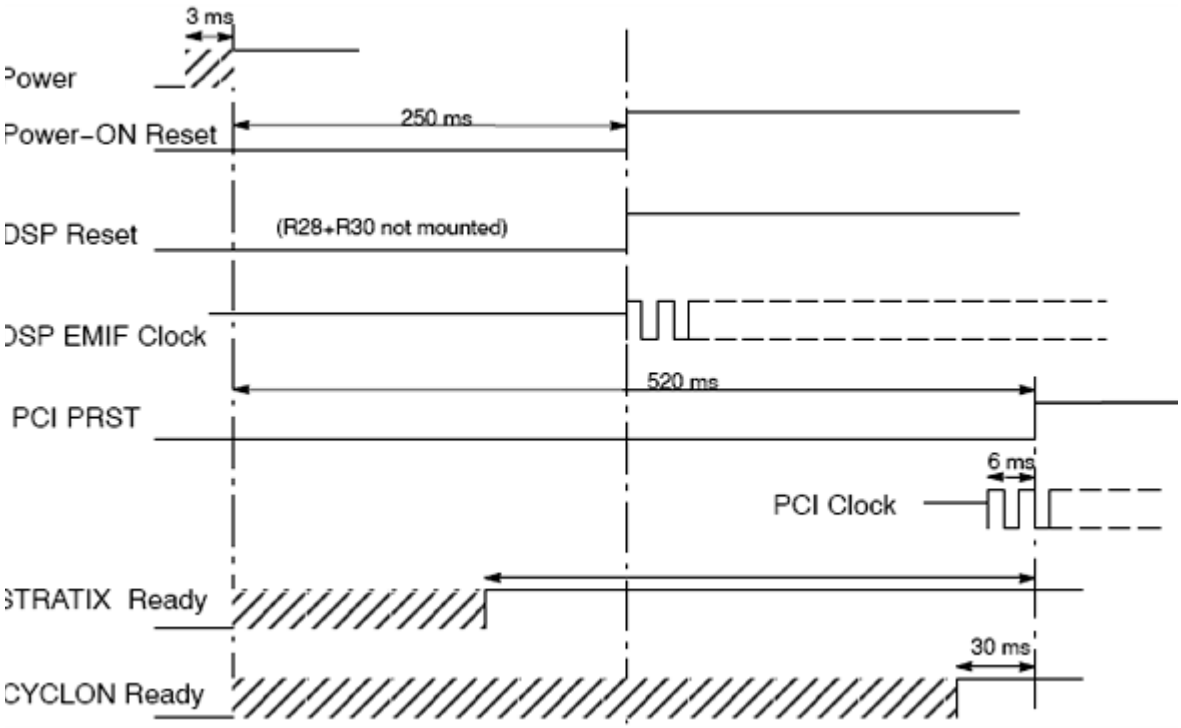


Figure 4.7: Power−On Reset Timing

Engineering Design *4.6*

IPSO Base Board of the IPSO 19” model, H12519

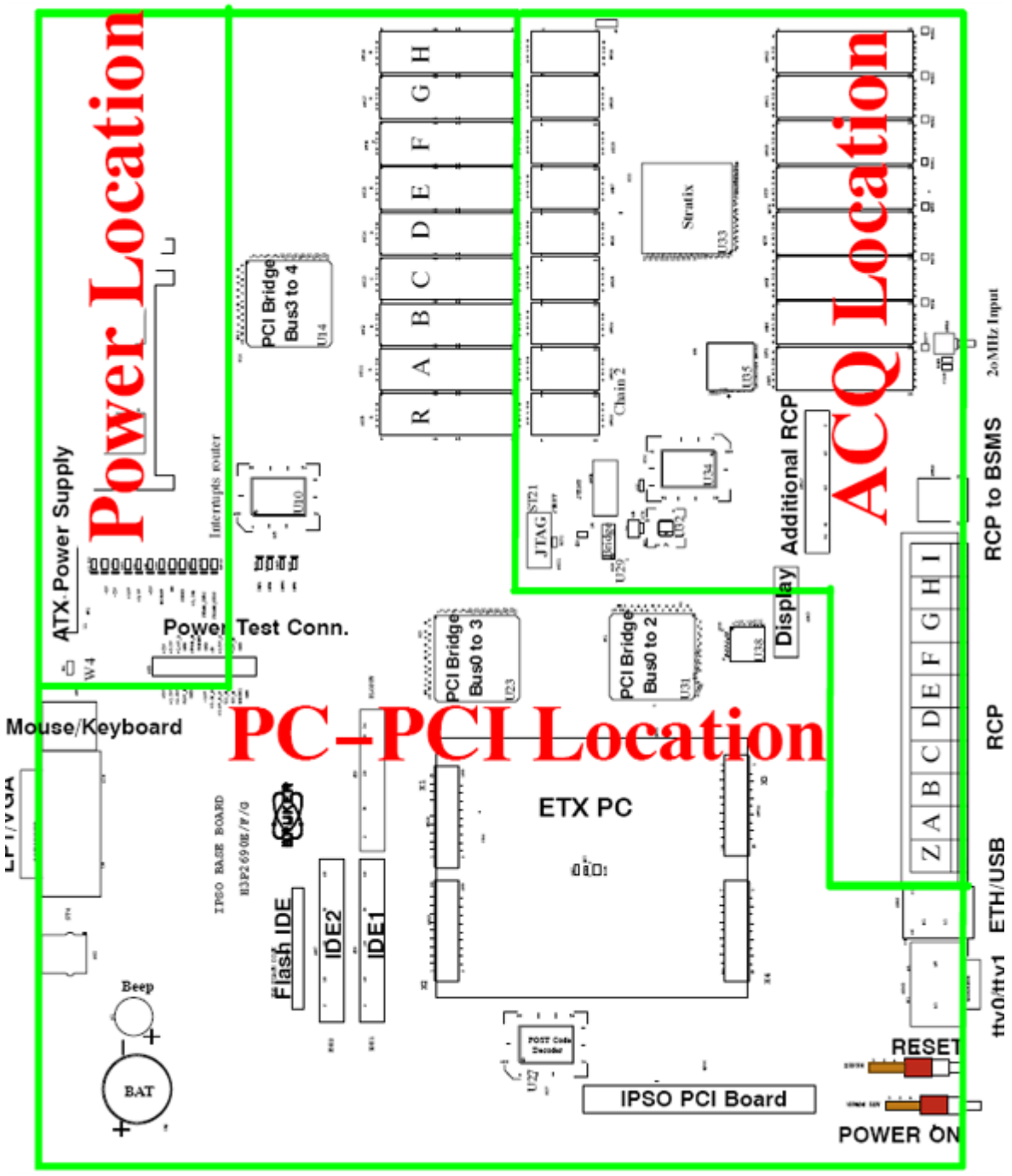


Figure 4.8: IPSO Base Board, H12519 and its connector locations

Ports 4.6.2

tty0/tty1 RS232 Interface

ETH 10/100 Mbit Ethernet Interface

USB USB 1.0; e.g. usable for Mouse and Keyboard

RCP Application specific Real Time Clock pulses 19 additional RCP signals without Coax locations are kept attachable at connector ST47 inside the 19“ case.

The pin assignment of RCP signals is included in chapter “1”.

Display Connector for Post Code Hex and LED devices

IPSO PCI B. Connector for the “Standard PCI Slot” adapter (H12524)

IDE Standard Interface to hard disks, if any. Hard disks are non-mandatory options.

Flash IDE Interface to a Flash−HD, if any. Flash HD is a non−mandatory option.

LPT PC Standard Parallel port

VGA PC Standard Interface for graphical monitors. A Monitor at IPSO is a non−mandatory option but necessary to check and modify the BIOS settings.

Mouse/Keyb. PC Standard PS/2 Mouse and Keyboard Interfaces

ATX Power PC Standard Power Supply Connector

JTAG Structure 4.6.3

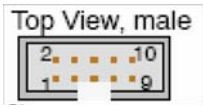


Figure 4.9: Pin Count of the JTAG Connectors

Table 4.31: JTAG Pre Bridge Connection (19U, H12519 ST21; AQS, H12547 ST20)

Pin Number	Signal	Pin Number	Signal
1	TRST*	6	JTAG Power +5 V
2	Cable Detection	7	TMS
3	TDO	8	GND

Table 4.31: JTAG Pre Bridge Connection (19U, H12519 ST21; AQS, H12547 ST20)

Pin Number	Signal	Pin Number	Signal
4	GND	9	TCK
5	TDI	10	GND

Table 4.32: JTAG connection after bridge (19U H12519 ST21; AQS H12547 ST19)

Pin Number	Signal	Pin Number	Signal
1		6	GND
2	Cable Detection	7	TMSL1
3	TDOL1	8	GND
4	GND	9	TCKL1
5	TDIL1	10	GND

Table 4.33: IPSO 19" Host, H12519 JTAG Structure

IC	JTAG Chain 1		JTAG Chain 2		JTAG Chain 3	
	IN	OUT	IN	OUT	IN	OUT
U33			TDIL2	TD2A		
U35			TD2A	TDOL2		
U14					TDIL3	TD3A
U10					TD3A	TD3B
U27					TD3B	TD3C
U23					TD3C	TD3D
U31					TD3D	TD3E
U38					TD3E	TDOL3

Table 4.34: Power Requirements of IPSO 19" Host, H12519

Part Number	Assembly		+5 V	Σ +5 V	+3.3 V	+12 V	+5 V SB	-12 V
H12519	IMB	ETX VIA 400 MHz + IMB		2.5 A	2.5 A	0.1	(1.8 A)	0.1
H12519	IMB	ETX PM 800 MHz + IMB		2.8 A	2.5 A	0.1	(1.66 A)	0.1

Connectors and Pin Allocation 4.7

PC Standard Interface Connectors 4.7.1

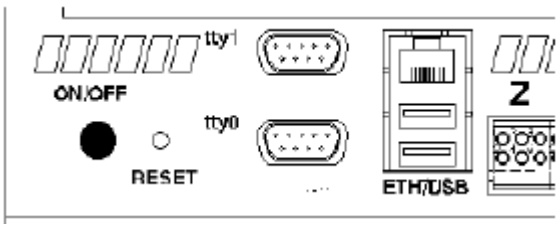
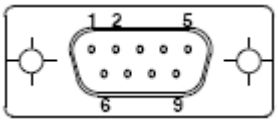


Figure 4.10: Location of the tty, ETH and USB Ports at the IPSO 19“ Unit

tty0 and tty1 ports (RS232)

Table 4.35: RS232 Signals of Ports tty0 and tty1, Male

RS232 Port tty0/tty1				
Pin	**Signal**	**Pin**	**Signal**	
1	DCD1	2	DSR1	
3	RXD1	4	RTS1	
5	TXD1	6	CTS1	
7	DTR1	8	RI1	
9	GND			

Combined Ethernet and USB Port connector

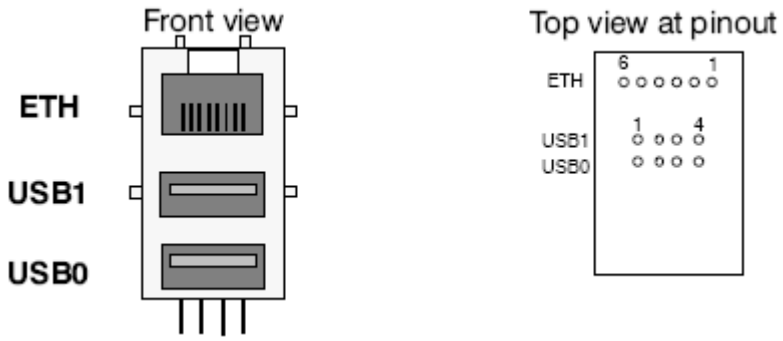


Figure 4.11: Combined Ethernet and USB Port Connector

Table 4.36: Ethernet Port

Ethernet Port Connector			
Pin Number	**Signal**	**Pin Number**	**Signal**
1		2	TxD+
3	TxD-	4	RxD+
5	RxD-	6	

Table 4.37: USB Connectors Signal Assignment

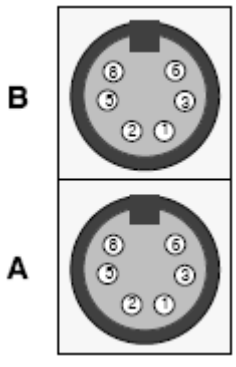
USB Port 0 Connector				USB Port 1 Connector			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	VCC_USB0	2	USB0-	1	VCC_USB1	2	USB1-
3	USB0+	4	GND_USB0	3	USB1+	4	GND_USB1

Keyboard, Mouse connectors (PS/2)

The location of these connectors is inside the IPSO case. Attaching a cable to them at the front panel is not possible. The IPSO AQS has to be pulled out of the rack and supplied with power by a standard ATX extension cable.

Table 4.38: Signal Assignment of the Keyboard and Mouse Connectors, Female

Keyboard Connector B				Mouse Connector A			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	KB_DAT	2		1	MS_DAT	2	
3	GND	5	VCC_KB	3	GND	5	VCC_KB
6	KB_CLK	8		6	MS_CLK	8	



Front View

Connectors of Parallel Port (LPT) and Analog Video output (VGA)

The location of these connectors is inside the IPSO case. Attaching a cable to them at the front panel is not possible. The IPSO AQS has to be pulled out of the rack and supplied with power by a standard ATX extension cable.

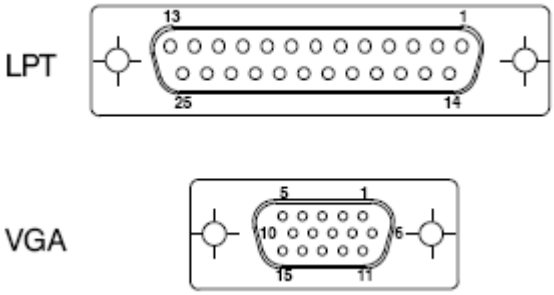


Figure 4.12: Parallel Port and VGA Connector, both Female

Table 4.39: Pin Assignment of Parallel Port and VGA Port

Parallel Port Connector			
Pin Number	**Signal**	**Pin Number**	**Signal**
1	STB#	2	AFD#
3	PA0	4	ERR#
5	PA1	6	INIT#
7	PA2	8	SLIN#
9	PA3	10	GND
11	PPA4	12	GND
13	PPA5	14	GND
15	PPA6	16	GND
17	PPA7	18	GND
19	ACK#	20	GND
21	BUSY#	22	GND
23	PE#	24	GND
25	SLCT#	26	GND

Analog Video (VGA) Port Connector			
Pin Number	**Signal**	**Pin Number**	**Signal**
1	ROUT	2	GOUT
3	BOUT	4	CK_DDC_OUT
5	GND	6	Shield
7	Shield	8	Shield
9	DDC_PWR	10	GND
11		12	DDC_DATA_OUT
13	HSYNC	14	VSYNC

IDE1, IDE2 Connectors

The location of these connectors is inside the IPSO case. Attaching a cable to them at the front panel is not possible. The IPSO AQS has to be pulled out of the rack and supplied with power by a standard ATX extension cable.

The Flash Disc connector is connected in the same way to the signals of Secondary IDE2. Its pin distance is 2mm instead of 0.1 inch.

Figure 4.13: Pin Count of the IDE Connectors

Table 4.40: Signal Assignment of IDE Connectors

Primary IDE1 Connector				Secondary IDE2/Flash IDE Connector			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	HDRST#	2	GND	1	HDRST#	2	GND
3	PIDE_D7	4	PIDE_D8	3	SIDE_D7	4	SIDE_D8
5	PIDE_D6	6	PIDE_D9	5	SIDE_D6	6	SIDE_D9
7	PIDE_D5	8	PIDE_D10	7	SIDE_D5	8	SIDE_D10
9	PIDE_D4	10	PIDE_D11	9	SIDE_D4	10	SIDE_D11
11	PIDE_D3	12	PIDE_D12	11	SIDE_D3	12	SIDE_D12
13	PIDE_D2	14	PIDE_D13	13	SIDE_D2	13	SIDE_D13
15	PIDE_D1	16	PIDE_D14	15	SIDE_D1	16	SIDE_D14
17	PIDE_D0	18	PIDE_D13	17	SIDE_D0	18	SIDE_D15
19	GND	20		19	GND	20	
21	PIDE_DRQ	22	GND	21	SIDE_DRQ	22	GND
23	PIDE_IOW#	24	GND	23	SIDE_IOW#	24	GND
25	PIDE_IOR#	26	GND	25	SIDE_IOR#	26	GND
27	PIDE_RDY	28		27	SIDE_RDY	28	
29	PIDE_AK#	30	GND	29	SIDE_AK#	30	GND
31	PIDE_INTR	32		31	SIDE_INTR	32	
33	PIDE_A1	34		33	SIDE_A1	34	

Table 4.40: Signal Assignment of IDE Connectors

35	PIDE_A0	36	PIDE_A2	35	SIDE_A0	36	SIDE_A2
37	PIDE_CS1#	38	PIDE_CS3#	37	SIDE_CS1#	38	SIDE_CS3#
39	PK5V	40	GND	39	SK5V	40	GND
				41	VCC (flash only)	42	VCC (flash only)
				43	GND (flash only)		

ATX Power connector

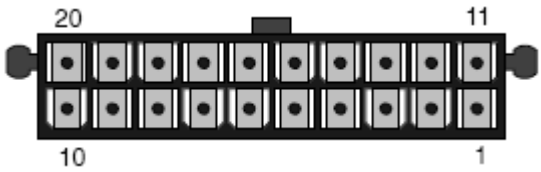


Figure 4.14: ATX Power Connector - Top View, Male Part

Table 4.41: ATX Power Supply Signal Assignment

Pin Number	Signal	Pin Number	Signal
1	3.3 V	11	3.3 V
2	3.3 V	12	-12 V
3	COM	13	COM
4	5 V	14	PS-ON
5	COM	15	COM
6	5 V	16	COM
7	COM	17	COM
8	PW-OK	18	-5 V
9	5 V SB	19	5 V
10	12 V	20	5 V

IPSO Power Test Connector

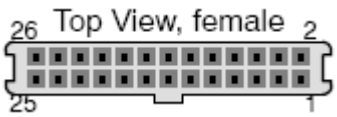


Figure 4.15: Power Test Connector - Top View, Female Part

Table 4.42: Power Test Connector ST5 Signal Assignment (IPSO 19” only)

Pin Number	Signal	Pin Number	Signal
1	+12 V	14	-12 V
2	+5 V	15	-5 V
3	+3.3 V	16	+3.3_DV
4	+1.5 V	17	+1.5_SV
5	1.4_DV	18	+1.4_D_SV
6	+2.5V	19	GND
7	GND	20	VCC_M
8	+12_MV	21	-12_MV
9	+5SBV	22	-5_MV
10	GND	23	GND
11	+USBPW	24	+USBPW1
12		25	
13	GND	26	GND

Tx Controller 5

Tx-Controller Versions 5.1

Location	Name	Part Number	ECL	Increments
IPSO 19”	IPSO Tx-controller, 2 MB, TMS320C6415	H12538F1	00	
IPSO 19”	IPSO Tx-controller, 2 MB, TMS320C6415	H12538F1	03	FIFO termination
IPSO 19”	IPSO Tx-controller, 16 MB, TMS320C6415	H12538F2	00	Deskew, 16 MB
IPSO 19”	IPSO Tx-controller, 128 MB, TMS320C6455	H12538F3	00	128 MB, TMS320C6455

Relevant Parts 5.2

Part Number 86868 LVDS Cable, 1m

Features 5.3

- The Tx-controller can be configured by software to fulfill one of three different tasks in the system:
  - as F-controller (FCtrl) generating the frequency parameter stream
  - as G-controller (GCtrl) generating the Gradient stream and
  - as T-controller (TCtrl) generating the RCP stream
- Each Tx-controller outputs a stream of 48−bit words at a clock rate of 80 MHz per word.
- Transfer of a complete set of frequency parameters requires two words.
- The time resolution of parameter switching in any combination of frequency, phase, amplitude is 12.5 ns.
- The minimal duration of any combination of parameters is 25 ns.
- Gradient channels require one word per gradient.
- The maximal number of addresses for different gradients (the max. number of gradient channels) is 1k.
- A constant time delay between the outputs of the different Tx-controllers may be adjusted to any number of 80 MHz clock cycles up to 2^{29} x 12.5 ns.

- The timing of each Tx-controller is controlled by its part of a sequencer.
- The sequencer parts of all Tx-controllers and their means of communication (AQ bus) are accommodated in one piece of silicon which is known as “The Sequencer”.

Operation *5.4*

The controller consists of a DSP with memory, FIFO, output logic and interfaces to the system bus and the sequencer. The DSP gets its code from the host controller, generates the parameter sequences and writes them into the FIFO. Its most important task is to keep the FIFO full. The Sequencer (once started) reads the words out of the FIFOs of all controllers, realizes the defined timing in each channel and controls the outputs.

The global functions of the sequencer (e.g. START, STOP, SUSPEND, RESUME and so on) are part of the sequencer logic of the T−controller. Therefore a T−controller has to be in the system to carry out any type of acquisition.

Architecture 5.5

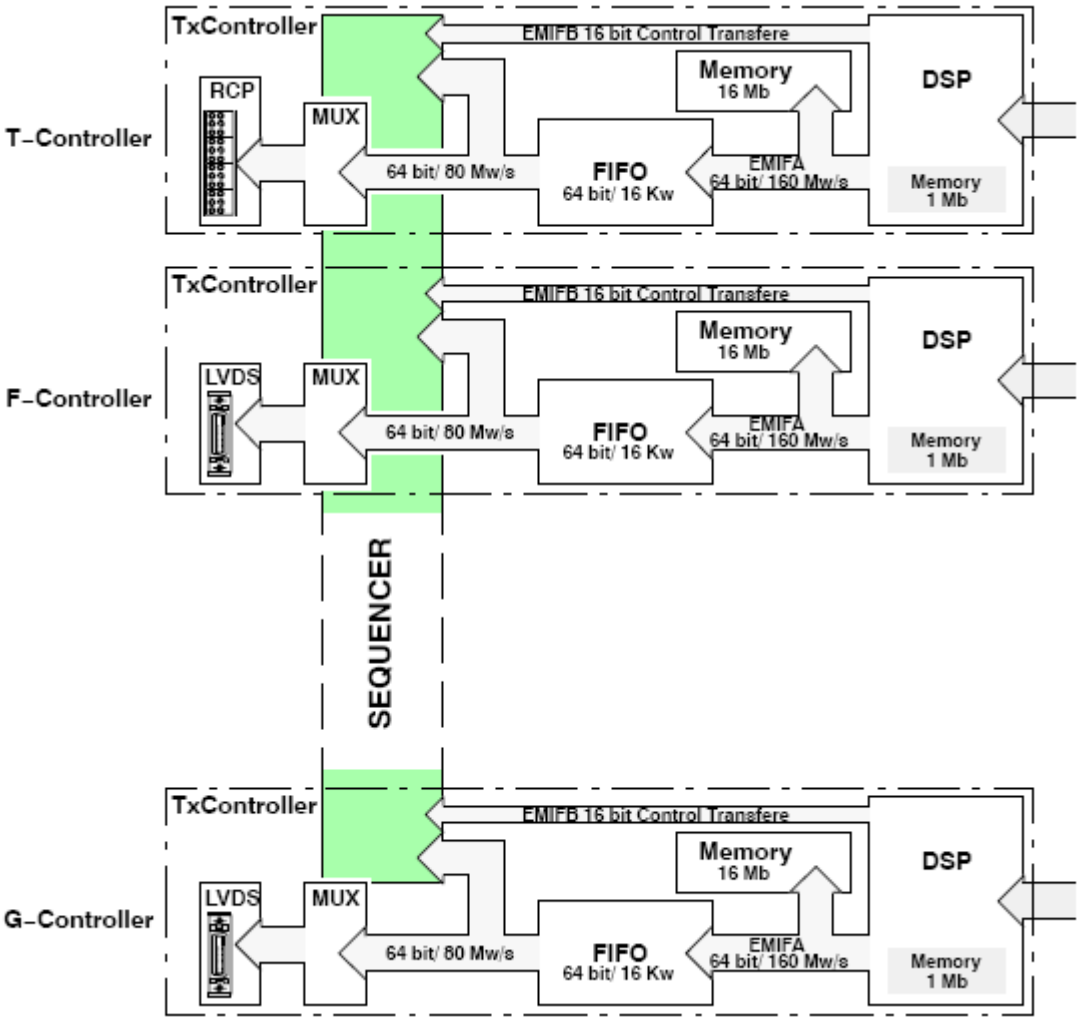


Figure 5.1: The Tx-Controller as T-, F- and G-Controller

Structure of Output Data 5.6

According to the respective task of the Tx-controller (as F-controller, G-controller or T-controller), the bits of the 64-bit FIFO words are combined in a different way and bear different information. In case of the T-controller, some of the FIFO bits control the RCP outputs at the coax connectors.

F-Controller 5.6.1

In the F-controller, a FIFO data set consists of two 64-bit words A+B. The bits 1 to 33 of the A-word hold the control and delay information of that channel needed by the “Sequencer”. The remaining bits of both words contain the control information for the “SGU”. These 96 bits are multiplexed to two 48-bit words which are transmitted back-to-back through the LVDS interface to the “SGU”.

FIFO Word Structure

Table 5.1: Word A in the FIFO of the F-Controller (64-Bit DSP -> FIFO Format)

Bit	64	...	55	54	53	...	38	37	36	35	34	33	32	...	2	1
Field	Register_Data REG 9...0			SH_ VAL	Amplitude SHAPE 15...0				free			OUT	Sequencer Control+Duration			A
Number	10			1	16				4			1	31			1

Table 5.2: Word B in the FIFO of the F-Controller (64-Bit DSP -> FIFO Format)

Bit	64	63	62	61	60	59	58	57	56	55	54	...	39	38	37	36	35	...	2	1
Field	REG_ VAL 1...0		PL S gat e	PA gat e	A gate	NCO_sel 2...0			PH_VA L 1...0		PHASE 15...0			F_VAL 2...0			F_DATA 33...0			B
Number	2			3		3			2		16			3			34			1

LVDS Word Structure

Table 5.3: Word A at the LVDS Interface (transfer FCTRL to SGU)

Bit	48	47	46	45	44	43	42	...	33	32	...	17	16	...	1

Table 5.3: Word A at the LVDS Interface (transfer FCTRL to SGU)

Field	PAR	SYN	WID	PLS	PA	A		REG 9...0		PHASE 15...0	SHAPE 15...0
Number	1	1	1		3			10		16	16

Table 5.4: Word B at the LVDS Interface (transfer FCTRL to SGU)

Bit	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	...	1
Field	PAR	SYN	WID	NCO_SEL 2...0			REG_VAL 1...0		F_VAL 2...0			PH_VAL 1...0		SH_VAL	F_DATA 33...0		
Number	1	1	1	3			2		3			2		1	34		

Table 5.5: Bit Fields of the F-controller Output Word

Field	Value	Description
F_DATA 33...0		34 bit frequency information.
SHAPE 15...0		16 bit amplitude information.
PHASE 15...0		16 bit phase information.
REG 9...0		10 bit register data.
PLS, PA, A		3 bit gate information.
SH_VAL		1 valid bit of amplitude information.
PH_VAL 1:0		2 valid bit of phase information.
F_VAL 2:0		3 valid bit of frequency.
REG_VAL 1...0		2 valid bit of register data.
NCO_SEL 2...0		3 select bits.
WORD_ID(WID)		Bit 46 in each word.
	0	Word A.
	1	Word B.
SYNCHRO		Reflects the current state of the 20−mhz reference clock at transmitter.
PARITY		The even parity bit, created from bit 1 to 46.

Idle State

The LVDS interface is continuously sending. In the idle state (if no valid words have to be transmitted) the interface sends repeatedly the default word “0x200000000007”.

Bit	48	47	46	45	44		43	42	...	33	32	...	17	16		...	1
Field	PAR	SYN	WID	Default Word of the idle state.													
Value	0	x	1	0 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111													

G-Controller *5.6.2*

In the G-controller, a FIFO data set can consists of two or more 64-bit words A + B1+ B2 + etc. The bits 1 to 33 of the A word hold the control and delay information of that channel needed by the “Sequencer”. The remaining B words contain the gradient data which are multiplexed to the 48-bit gradient words and transmitted through the LVDS interface to the gradient amplifier.

Either gradient words contain a NG bit (!NG=0) and no data (!VALID=1) or data (!VALID=0) and no NG (!NG=1). The word with the NG bit sets the time at which all the gradient data, transferred since the previous NG, will be active.

FIFO Word Structure

Table 5.6: A-Word at FIFO Output

Bit	64	...	35	34	33	32	...	2	1
Field	reserved			NG	OUT	Sequencer Control+Duration			A/B
Number	30			1	1	31			1

Table 5.7: B-Word at FIFO Output

Bit	64	...	48	47	...	44	43	...	38	37	...	22	21	...	18	17	...	6	5	4	3	2	1
Field	reserved			MSB Address			MSB Data									Data (res.)			res.		LAST	VALID	A/B
				ADD<9...6>			ADD<5...0>			DATA <19...0>						gnd			gnd				
Number	17			4			6			16			4			12			1	1	1	1	1

Table 5.8: Gradient Word at LVDS Interface, 48 Bit, 80 MHz

Bit	48	47	..	44	43	..	38	37	. .	22	21	. .	18	17	...	6	5	4	3	2	1
Field	PAR	MSB Address						MSB Data						Data (res.)			res.		!LAST	!VALID	!NG
		ADD<9...6>			ADD<5...0>			DATA <19...0>						gnd			gnd				
Number	1	4			6			16			4			12			1	1	1	1	1

Table 5.9: Bit Fields of the G-Controller Words

Field	Value	Description
A/B	0 1	Word ID. A−Word. B−Word.
OUT	1 0	Sequencer Information. Means that the following B words contain data which has to be transferred via the LVDS (NG = 1 or Valid = 1). OUT is high active. No transmit of A or B content via LVDS; only bit 1 to 33 of A word contain valid information.
!NG	0 1	Next Gradient Bit, High Active in FIFO, Low Active at LVDS interface. This A word generates a gradient word which contains NG only, no data (!VALID=1). This word must contain !VALID = 0 and gradient data.
!VALID	0 1	Gradient Data Valid−Bit; High−Active in FIFO, Low−Active at LVDS−Interface This word contains Gradient data and no “Next Gradient”; !NG=0 in the same word would be a fatal error. No Gradient data in this word.
PAR		Parity bit; Even Parity of Bit1 to 47.
!LAST	0	Indicates the last word of the gradient data set with !NG = 0 or !VALID = 0; High-Active in FIFO, Low-Active at LVDS-interface.

Idle State

The LVDS interface is continuously sending. In the idle state (if no valid words have to be transmitted) the interface sends repeatedly the default word “0x200000000007” with valid and NG not active.

Bit	48	47	46	45	44	43	42	...	33	32	...	17	16	...	1

Field	PAR	SYN	WID			Default Word of the Idle State
Value	0	x	1			0 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111

T-Controller *5.6.3*

In the T-controller, a FIFO data set consists of two 64-bit words A+B. The bits 1 to 33 of the A word hold the control and delay information of that channel needed by the “Sequencer”. The remaining bits of both words contain the control information for the RCP signals.

High = 5 Volts

Low = 0 Volts

These 67 bits of “setnmr 0, 3 and 4”are connected to the coax-outputs and gain control at the same time FIFO word structure.

Table 5.10: FIFO A-Word

Bit	64	63	62	61	60	59	58	57	...	36	35	34	33	32	...	2	1
Field		res		setnmr0 (34,33,32)			setnmr4 (31)		res		free		OUT	Sequencer Control + Duration			A/B
Number			6				1		22		2		1	31			1

Table 5.11: FIFO B-Word

Bit	64		34	33		2	1
Field		setnmr4 (30...0)			setnmr3 (31...0)		A/B
Number		31			32		1

Table 5.12: Control Fields of the T-Controller FIFO Words

Field	Value	Description
OUT		Sequencer information.
	1	Means that the RCP outputs will be updated with the state of the setnmr bits.
		(OUT is “High” active in the FIFO).
	0	No update of the RCP outputs.

Software Interface 5.7

All resources of the Tx-controller except the FIFO can be accessed by the software running local on the DSP or by the software that runs on the host controller via the PCI bus. Due to the 32-bit interface of the PCI bus the FIFO is accessible only by the DSP.

Both address rooms (DSP + host-controller) are spanned by 32-bit addresses. An address window into the address room of each DSP is arranged in the address room of the Host-controller. The arrangement of these windows is defined by the PCI base register and the DSP page register of each DSP.

PCI Addresses 5.7.1

The content of the base register (<Base>) is defined by the BIOS of the host controller.

The content of the DSPP registers (<DSPP>) defines the software running on the host controller. The DSPP register is accessible via the nonprefetchable range.

Table 5.13: Relation Between PCI Addresses and Local Addresses

	4 MByte Prefetchable Range		8 MByte Nonprefetchable Range	
	Bit [31...22]	**Bit [21...0]**	**Bit [31...23]**	**Bit [22...0]**
PCI Address	<Base0>	AD [21 0]	<Base1>	AD [22 0]AD [22...0]
Local Address	<DSPP>	AD [21...0]	0000 0001 1	

Local Address Layout 5.7.2

Table 5.14: Memory Map of the DSP 6415

Local Hex Address Range	Block Size (Bytes)	Bus	Data Bus Width (Bytes)	Description	Utilization
180 0000 − 0183 FFFF	256 K	Internal	8	On-chip RAM	
0184 0000 − 0187 FFFF	256 K	Internal		EMIFA Config. Register	
0194 0000 − 0197 FFFF	256 K			Timer 0 Register	
0198 0000 − 019B FFFF	256 K			Timer 1 Register	

Table 5.14: Memory Map of the DSP 6415

019C 0000 − 019F FFFF	256 K			Interrupt Select Register	
01A0 0000 − 01A3 FFFF	256 K			Enhanced DMA Register	
01A8 0000 − 01AB FFFF	256 K	Internal		EMIFB Config. Register	
01AC 0000 − 01AF FFFF	256 K	Internal	Timer 2 Register		
01B0 0000 − 01B3 FFFF	256 K	Internal		GPIO Register	
01C0 0000 − 01C3FFFF	256 K			PCI Register	
6000 0000 − 63FF FFFF	64 M	EMIFB CE0	2	External RAM	Register
6400 0000 − 67FF FFFF	64 M	EMIFB CE1	2	External RAM	Register
6800 0000 − 6BFF FFFF	64 M	EMIFB CE2	2	External RAM	BIS Flash Prom
6C00 0000 − 6FFF FFFF	64 M	EMIFB CE3	2	External RAM	
8xxx xxxx	256M	EMIFA CE0	8	External RAM	RAM
9xxx xxxx	256M	EMIFA CE1	8	External RAM	FIFO 16Kx64
Axxx xxxx	256M	EMIFA CE2	8	External RAM	
Bxxx xxxx	256M	EMIFA CE3	8	External RAM	

Content of the DSP Configuration Registers *5.7.3*

Table 5.15: EMIFA Configuration Register

Local Hex Address	Acronym	Value	Description
1800048	CE0SEC	00000042	EMIFA CE0 Space Secondary Control.
1800044	CE1SEC	00000060 00000064	EMIFA CE1 Space Secondary Control. Tx-Controller with 2 MByte SRAM. Tx-Controller with 16 MByte SDRAM.

Table 5.15: EMIFA Configuration Register

1800050	CE2SEC	Unmodified	EMIFA CE2 Space Secondary Control.
1800054	CE3SEC	Unmodified	EMIFA CE3 Space Secondary Control.
1800000	GBLCTL	00012024 00010034	EMIFA global Control. Tx-Controller with 2 MByte SRAM. Tx-Controller with 16 MByte SDRAM.
1800008	CE0CTL	FFFFFFE3 FFFFFFD3	EMIFA CE0 Space Control. Tx-Controller with 2 MByte SRAM. Tx-Controller with 16 MByte SDRAM.
1800004	CE1CTL	FFFFFFE3	EMIFA CE1 Space Control.
1800010	CE2CTL	FFFFFFB3	EMIFA CE2 Space Control.
1800014	CE3CTL	FFFFFFB3	EMIFA CE3 Space Control.
1800018	SDCTL	0248f000 47228000	EMIFA SDRAM Control Tx-Controller with 2 MByte SRAM Tx-Controller with 16 MByte SDRAM.
180001C	SDTIM	00000000 0000094C	EMIFA SDRAM Refresh Control Tx-Controller with 2 MByte SRAM Tx-Controller with 16 MByte SDRAM
1800020	SDEXT	00175F3F 0005052B	EMIFA SDRAM Extension Tx-Controller with 2 MByte SRAM Tx-Controller with 16 MByte SDRAM.

Table 5.16: EMIFB Configuration Register

Local Hex Address	Acronym	Value	Description
1A80000	GLBCTL	00012024	EMIFB global Control
1A80008	CE0CTL	5055C11D	EMIFB CE0 Space Control, Register
1A80004	CE1CTL	5055C11D FFFFFFBF	EMIFB CE1 Space Control, Register on TCTRL on FCTRL and GCTRL
1A80010	CE2CTL	2A22E80A	EMIFB CE2 Space Control, BIS Flash Prom
1A80014	CE3CTL	FFFFFFBF	EMIFB CE3 Space Control, not used.

Table 5.17: GPIO Configuration Register

Local Hex Address	Acronym	Value	Used As	Description
01B00000	GPEN	0x1FF		GPIO Bit Enable; Usage of the GPIO Pin GP0,...,GP8 as IO Pin
01B00004	GPDIR	0xE 0 – – – 1 -> 0 1 -> 0 1 -> 0 1 -> 0	 SGU Status “Ask me”, not applied not applied not applied DSP EXT_INT4 Sequencer Error Interrupt. DSP EXT_INT5 Emergency Stop Interrupt. DSP EXT_INT6 FIFO almost empty, the FIFO contains less than 33 words. DSP EXT_INT7 FIFO almost full, the FIFO can accept less than 31 words.	Direction of GPIO Pins adjusted as: GP0 Input on TCTRL, not applied on F− and GCTRL. GP1 Output. GP2 Output. GP3 Output. GP4 Input. GP5 Input. GP6 Input. GP7 Input.
		0	Emergency Stop active.	GP8 Input on TCTRL, not applied on FCTRL and GCTRL.
01B00008	GPVAL	0xFF		GPIO Value Register, Output Value of GPIO.

Memory at EMIFA *5.7.4*

Table 5.18: Type of External Memory Used on the Tx-Controllers

Local Hex Address	Size (MBytes)	Word (Bytes)	Type	Bandwidth (MBytes)	Type of Controller	Identification
8000 0000 - 801F FFFF	2	8	SRAM	1280	TxCtrl H12538	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX
8000 0000 - 80FF FFFF	16	8	SDRAM	1280	TxCtrl H12538F1 H12538F2 AQS-ACQ H12549	imbf=FFFF or 0000 and slot_brdv=XFXX or X1XX imbf=0001 and t_brdv=0000

FIFO at EMIFA 5.7.5

The FIFO is filled by the DSP using the signal CE1 and address “0x9xxx xxx”. Its content is read by the sequencer.

Table 5.19: Type of FIFOs Used on the Tx-Controllers

Local Hex Address	Size (KBytes)	Word (Bytes)	Type	Bandwidth (MBytes)	Type of Controller	Identification
9xxx xxxx	128	8		1280	TxCtrl H12538 TxCtrl H12538F1 H12538F2 AQS-ACQ H12549	slot_brdv=XFXX or X0XX slot_brdv=X1XX t_brdv=0000

Flash Prom on the EMIFB Bus 5.7.6

EMIF bus properties accessing the BIS Flash Prom:

Bus Width: 2 byte, data bit 7...0 implemented, data bit 15...8 not implemented, therefore the Prom occupied the double address room.

Cycle Operation: Synchronal

Cycle Duration: Circa 85 nsec for the write cycle and 270 nsec for the read cycle.

Table 5.20: Type of Flash Proms Used on the Tx-Controllers

Local Hex Address	Size (KBytes)	Word (Bytes)	Type	Type of Controller	Identification
6800 0000 - 6801 FFFF	64	1		TxCtrl H12538 TxCtrl H12538F1 H12538F2	slot_brdv=XFXX or X0XX slot_brdv=X1XX
6800 0000 - 6801 FFFF	64	1		AQS-ACQ H12549	t_brdv=0000

Registers on the EMIFB Bus *5.7.7*

All registers of the Tx-controller itself and its registers inside the sequencer are serviced via the EMIFB with following properties:

Bus Width: 2 Byte, data bit 15...0.

Cycle Operation: Asynchron, ready controlled.

Cycle Duration: About 144 nsec for the write cycle and 120 nsec for the read cycle.

Address Layout on EMIFB space CE0: Common Control Register

Table 5.21: Control Registers Common on F, G, and T-Controllers, EMIFB, Space CE0

Acronyms	Local Address	Function	Mode R/W	Bit
rtrig	60000000	External trigger and FIFO output	R	15-0
mflag	60000004	Flag register (LFLG, FFLG, MFLG)	W	2-0
fifores	60000008	FIFO reset control	W	xxxx
seqsts	6000000C	Sequencer & FIFO status register	R	15-0
delaya	60000010	Write/read delay register A	W/R	15-0
delayb	60000014	Write delay register B	W	15-0
seqlst	60000018	Sequencer local start	W	xxxx
seqres	6000001C	Reset of the sequencer	W	xxxx
seqctl	60000020	Sequencer interrupt control register	W	8-0
seqint	60000024	Sequencer interrupt register	W/R	15-0
rcpout	60000028	Enable/disable RCP output	W	Bit 0
fpgavsn	6000002C	Version of FPGA	R	15-0
chanconf	60000030	Channel configuration	R	15-0
slot_brdv	60000038	Slot and board version of FCtrl/GCTRL	R	15-0

Table 5.22: Control Registers on F and G-Controllers, EMIFB, Space CE0

Acronyms	Local Address	Function	Mode R/W	Bit
selfg	60000034	Select GCtrl or FCtrl function.	W	0

Table 5.22: Control Registers on F and G-Controllers, EMIFB, Space CE0

semif	60000058	Select FIFO or register set to LVDS output.	W	0
dstrb	6000005C	Generate data valid strobe.	W	x
srgs	600000A4	Select register set for read back.	W	0
NGS	60000060	Generate next gradient signal.	W	x
goutA	60000064	Bypass register A.	R/W	15-0
goutB	60000068	Bypass register B.	R/W	15-0
goutC	6000006C	Bypass register C.	R/W	15-0
foutD	60000098	Bypass register D.	W	15-0
foutE	6000009C	Bypass register E.	W	15-0
foutF	600000A0	Bypass register F.	W	15-0
lvds_dsk	600000A8	LVDS Deskew.	R/W	1-0

Address Layout on EMIFB space CE0: RCP Output Register and Version Register

Table 5.23: RCP Output and Version Registers on T-Controller, EMIFB, Space CE0

Acronyms	Local Address	Function	Mode R/W	Bit
t_brdv	6000003c	Board version of IPSO AQS ACQ.	R/−	15−0
rcpout	60000028	Disable/enable RCP outputs.	−/W	0
tout4	60000040	TCtrl output register 4.	R/W	5−0
tout3	60000044	TCtrl output register 3.	R/W	15−0
tout2	60000048	TCtrl output register 2.	R/W	15−0
tout1	6000004C	TCtrl output register 1.	R/W	15−0
tout0	60000050	TCtrl output register 0.	R/W	15−0
selrcp	60000054	Select FIFO or tout registers as RCP source.	−/W	0
fpgavsn	6000002C	Read version of sequencer FPGA.	R/−	15−0

Address Layout on EMIFB space CE1: AQ Bus Control Register and Spin Rotation Counter Control

Table 5.24: RCP Output and Version Registers on T-Controller, EMIFB, Space CE0

Acronyms	Local Address	Function	Mode R/W	Bit
seqstart	64000078	Start the sequencer.	-/W	xxxx
seqstop	6400007C	Stop the sequencer.	-/W	xxxx
aqst_clr	64000074	Release AQSTART (sequencer stop).	-/W	xxxx
seqsus	64000080	Suspend of the sequencer.	-/W	xxxx
seqrsm	64000084	Resume of the sequencer.	-/W	xxxx
sustrig	64000088	Select trigger for suspend.	-/W	2-0
synctrig	6400008C	Synchronize trigger with the next-value clock.	-/W	3-0
lgcnt	64000090	Load next-value counter.	-/W	15-0
emstop	64000070	Set emergency stop.	-/W	Bit 0
reserve gl_chanconf	64000094	Read Gl. channel configuration temp. currently not used.	R/-	15-0
srtrsel	640000AC	Spin rotation trigger select.	-/W	3-0
srcen	640000B0	Spin rotation counter enable. read sr_counter control signal.	W R	Bit 0 15-0
src1lo	640000B4	Read spin rotation counter 1 lower word .	R	15-0
src2	640000B8	Read/write spin rotation counter 2.	R/W	15-0
src1hi	640000BC	Read spin rotation counter 1 upper word.	R	15-0

Registers of Common Use on all TxCtrl-Functions *5.7.7.1*

Register Description: Control Registers on EMIFB, space CE0

Table 5.25: Read External Trigger (rtrig)

Acronyms	Local Address	Function	Mode R/W	Bit
rtrig	60000000	Read external trigger and FIFO output.	R	15-0

TRIG1-4 are the external trigger signals. Their state can be checked by access to these registers.

Bit 4 to Bit 15 are used by the test software only. The FIFO/WID and the FIFO outputs Bit 21 to Bit 31 can be read via these bits.

Bit	15		5	4	3	2	1	0
Field	FIFO Data Out Bit 31 - Bit 21			FIFO Word ID	TRIG 4	TRIG 3	TRIG 2	TRIG 1

Table 5.26: Sequencer Flag Register (mflag)

Acronyms	Local Address	Function	Mode R/W	Bit
mflag	60000004	Flag Register (LFLG, FFLG, MFLG)	W	2-0

The register contains the flags which define the functional priority and dependency of this channel.

The state of these flags can be read via 0x6000000C.

Bit	15		3	2	1	0
Field	Not implemented.			MFLG	FFLG	LFLG
Reset State				0	0	0

Table 5.27: Sequencer Flag Register

Field	Value	Description

Table 5.27: Sequencer Flag Register

MFLG FFLG LFLG		Master flag. First flag. Last flag. Configured as master (111), a channel can only be reconfigured by changing the Flags with subsequent 'SEQRES'. These flags are not cleared by 'SEQRES'. After power-up are all flags = 0 (slave)
MFLG FFLG LFLG	000 001 010 011 100 101 110 111	Slave controller. Its delay register contains a greater value as the master controller. Last slave controller. With largest delay register content. Illegal code. Illegal code. Independent controller. Its delay register contains the same value as the master controller. Independent but for wait. Its delay register contains the same value as the master controller. A wait is finished by the last slave. Master controller when there are not slaves in the system. Master controller with dependent slaves.

Table 5.28: FIFO Reset Device Code (fifores)

Acronyms	Local Address	Function	Mode R/W	Bit
fifores	60000008	FIFO Reset Control	W	xxxx

Writing to this address (no data) clears the internal FIFO counters and the FIFO Flag Logic (= clear of contents)

Table 5.29: Sequencer & FIFO Status Register (seqsts)

Acronyms	Local Address	Function	Mode R/W	Bit
seqsts	6000000C	Sequencer & FIFO Status Register	R	15-0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields																

Table 5.30: Sequencer and FIFO Status Register

Field	Value	Description
Bit15		Master flag, MFLG
Bit14		First flag, FFLG
Bit13		Last flag, LFLG
Bit 12	 0 1	FIFO output ready. Output ready to be read, FIFO contains at least one word. FIFO empty.
Bit11	 0 1	FIFO half full flag. FIFO contains more than 4096 words. FIFO contains less than 4096 words
Bit10	 0 1	PAE, flag of FIFO almost empty. Threshold adjusted to 32 words. FIFO contains less than 33 word, EXT_INT6 of the DSP is activated. FIFO contains more than 32 words.
Bit9	 0 1	PAF, flag of FIFO almost full. Threshold adjusted to 31 words. The FIFO can accept less than 31 further words, EXT_INT7 of the DSP is activated. The FIFO can accept more than 31 further words.
Bit8	 0 1	FIFO input ready. Input ready, FIFO not full. FIFO full.
Bit7	 0 1	State of the AQSTART signal of the AQ bus. Since setting the Start−FF can be synchronized with the Next−Value Clock, bit 7=0 can be delayed after seqstart by a full clock period (at least 1 microseconds). AQSTART active, Start−FF set. AQSTART inactive, Start−FF reset.
Bit6	 0 1	SLEEP_ST, controller specific sleep state after reading of a sleep instruction. Awake. Sleeping.
Bit5	 0 1	Stop window signal of the AQ bus. Stop window set. The master controller has halted and calls on all slaves to stop at the next stop instruction. No stop from master.
Bit4	 0 1	Decision window signal of the AQ bus. Decision window set. The master controller has decided on IF or ELSE, shows the result with bit 3 and calls on all slaves to do the same at their next IF/ELSE instruction. No decision from master.
Bit3	 0 1	IF/ELSE signal of the AQ bus showing the master's decision. Decision for IF. Decision for ELSE.

Table 5.30: Sequencer and FIFO Status Register

Bit2	0 1	Controller specific WAIT status after reading a WAIT instruction. No WAIT. WAIT.
Bit1	0 1	Suspend−Window signal of the AQ Bus. The master controller has gone into the suspend mode (halted) and calls on all slaves: - to stop at their next SUSPEND instruction, - to set Bit0=1 of this register, - to set the DSP interrupt EXT_INT4. No suspend situation.
Bit0	0 1	Controller specific suspend status. No suspend. Suspend.

Table 5.31: Sequencer Delay Register (delaya, delayb)

Acronyms	Local Address	Function	Mode R/W	Bit
delaya	60000010	Write/read delay register A	W/R	15-0
delayb	60000014	Write/read delay register B	W	12-0

The content of the delay counter defines the independent start delay of this channel in steps of 12.5 nsec. The maximal delay is 6.5 sec. The counter contains 29 bits. Therefore, the two register locations A + B are required to write to the counter.

Register A can also be read to provide a test facility.

Bit	15	14	13	12		0	15		0
Field	Not used			Register B			Register A		
	Not used			29 Bit Delay Register					

Table 5.32: Sequencer Local Start Device Code (seqlst)

Acronyms	Local Address	Function	Mode R/W	Bit
seqlst	60000018	Sequencer local start.	W	xxxx

Writing to the “Sequencer Local Start” address (no data) puts this sequencer part from IDLE to RUN and enables this channel to follow the global acquisition start instruction „AQSQSTART”.

After Power-up, reset or in case of an error interrupt, the sequencer part of this channel enters the IDLE state and any AQSTART is cleared. Resuming the normal operation requires “selqst” in each channel followed by “AQSTART”.

Table 5.33: Sequencer Reset Device Code (seqres)

Acronyms	Local Address	Function	Mode R/W	Bit
seqres	6000001C	Reset of the sequencer.	W	xxxx

Writing to the “Sequencer Reset” address (no data) puts this sequencer part from RUN to IDLE state and disables this channel to follow the global acquisition start instruction “AQSTART”. The operating duration and the control and status register of this channel are cleared.

Resuming the normal operation requires “selqst”.

AQSTART is not affected by “seqres”.

Table 5.34: Control of Sequencer RUN/IDLE

Field	Value	Causal Event	Condition	Description
Local SEQ	IDLE -> RUN	Write to seqlst.	-	Sequencer part of this channel enabled for AQSTART.
	RUN -> IDLE	Write to seqres. Write to seqres. Write to seqstop. Write to aqst_clr Reset	-	Sequencer part of this channel disabled for write to seqstop AQSTART.

Table 5.35: Sequencer Interrupt Control Register (seqctl)

Acronyms	Local Address	Function	Mode R/W	Bit
seqctl	60000020	Write sequencer interrupt control register.	W	8-0

This register operates as the interrupt mask register for interrupts 0 to 8. Set to “high” enables the respective source to interrupt the DSP.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Not used.							Int 8	Int 7	Int 6	Int 5	Int 4	Int 3	Int 2	Int 1	Int 0
Reset State	Not used.							0	0	0	0	0	0	0	0	0

Table 5.36: Sequencer Interrupt Control Register

Field	Value	Description
Interrupt 0	1	Programmed Interrupt (high active).
Interrupt 1	1	STOP Interrupt (high active).
Interrupt 2	1	Illegal Instruction Interrupt.
Interrupt 3	1	Illegal configuration of the channel.
Interrupt 4	1	Suspend Interrupt.
Interrupt 5	1	ILLEGAL WORD Interrupt.
Interrupt 6	1	Empty FIFO Interrupt.
Interrupt 7	1	IF_ELSE Interrupt.
Interrupt 8	1	Error Interrupt nested if else sequence.

Table 5.37: Sequencer Interrupt Register (seqint)

Acronyms	Local Address	Function	Mode R/W	Bit
seqint	60000024	Write/read sequencer interrupt status register.	W/R	15-0

The register shows the state of the interrupt sources. An interrupt is active if the corresponding bit is high.

The sources of bit 0 to 8 activate the EXT_INT4 (GP4) of the DSP if the respective bit in the “Sequencer Interrupt Control Register” is set.

Writing a “1” to any of these bits clears the state of the corresponding source.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Int_Vec				Int 11	Int 10	Int 9	Int 8	Int 7	Int 6	Int 5	Int 4	Int 3	Int 2	Int 1	Int 0

Table 5.38: Sequencer Interrupt Status Register

Field	Value	Description
Interrupt 2	1	Illegal instruction interrupt.
Interrupt 3	1	Illegal configuration of the channel.

Table 5.38: Sequencer Interrupt Status Register

Interrupt 4	1	Suspend interrupt.
Interrupt 5	1	ILLEGAL WORD Interrupt.
Interrupt 6	1	Empty FIFO Interrupt.
Interrupt 7	1	If_ELSE Interrupt.
Interrupt 8	1	Error interrupt nested IF_ELSE sequence.
Interrupt 9	x	Unused.
interrupt 10	1	Programmed stop status (high active).
Interrupt 11	1	AQSTOP error status (high active).
Int_Vec Bit 12	1	Programmable interrupt vector Bit(0) (high active).
Int_Vec Bit 13	1	Programmable interrupt vector Bit(1) (high active).
Int_Vec Bit 14	1	Programmable interrupt vector Bit(2) (high active).

Table 5.39: Read Channel Configuration Register (chanconf)

Acronyms	Local Address	Function	Mode R/W	Bit
chanconf	60000030	Channel configuration.	R	15-0

The bits of the “Channel Configuration Register” provide information about the version of the installed controller, its function and mounting option.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Board function			Version						FCTRL channel			External configuration bit			

Table 5.40: Channel Configuration Register

Field	Value	Description
External Config. Bits		Details of “Board Function”:
		On F−controller and G−controller:
		Bit 0 and 1 provide the type of the device connected via LVDS. Bit 2 and 3 are reserved.
	xx00 xx01 xx10 xx11	DPP connected GCUTYPE = 11. SGU connected. Gradient amplifier connected GCUTYPE = 10. Nothing connected. On T−controller of IPSO AQS ACQ: Bit 0 and 1 provide the type of installed RCP adapter (HR or FTMS). Bit 2 and 3 are unused.
	xx00	Reserved.
	xx01	ACQ with FTMS Adapter.
	xx10	ACQ with HR Adapter (for NMR applications).
	xx11	No adapter.
FCtrl Channel		Provides the channel number 1 to 8 of this FCtrl. On TCtrl and RCtrl is the FCtrl Channel = 0. GCtrl takes a subsequent number.
	111 110 101 100 011 010 001 000	F−Controller 1. F−Controller 2. F−Controller 3. F−Controller 4. F−Controller 5. F−Controller 6. F−Controller 7. F−Controller 8 or TCtrl, RCtrl.

Table 5.41: Slot Board Version Register from FCTRL, GCTRL or TCTRL (slot_brdv)

Acronyms	Local Address	Function	Mode R/W	Bit
slot_brdv	60000038	PCI slot and board version of a Tx-controller	R	15-0

The register contains the slot address and the hardware version of a Tx-controller.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Slot Address				Board revision				Board sub-revision							

Table 5.42: Slot Board Version Register

Field	Value	Description
Board Revision	0000 0001 0002	IPSO−TX with 2MB external RAM + TMS320C6415; H12538F1. IPSO−TX with 16MB external RAM + TMS320C6415; H12538F2. IPSO−TX with 128MB external RAM + TMS320C6455; H12538F3.
Board Sub-revision	00000000	8 bit number for future use.
Slot Add		Slot address of this controller.
	0001	Slot 1.
	0010	Slot 2.
	0011	Slot 3.
	0100	Slot 4.
	0101	Slot 5.
	0110	Slot 6.
	0111	Slot 7.
	1000	Slot 8.
	1001	Slot 9.

Registers Used on F-Controllers and G-Controllers *5.7.7.2*

Register Description: Output Control Register on EMIFB, Space CE0

Table 5.43: Select GCTRL or FCTRL Function (selfg)

Acronyms	Local Address	Function	Mode R/W	Bit
selfg	60000034	Select GCtrl or FCtrl function.	W	0

1-bit register for configuration of this Tx-controller as F-controller or G-controller. This register is not affected by the sequencer reset.

Field	Value	Description
		The state is indicated by a LED at the front panel below the LVDS connector. Default after power−up is bit<0> = 0: FCtrl.
Write to Bit 0	0	Command cff: Tx as F−controller. LED = green.
	1	Command cfg: Tx as G−controller. LED = orange.

Table 5.44: Select FIFO or EMIF-Bypass Registers to Feed the LVDS (semif)

Acronyms	Local Address	Function	Mode R/W	Bit
semif	60000058	Select FIFO or register to become source of the LVDS output.	W	0

1-bit register switching the LVDS output from FIFO to a set of registers (gout, fout) and vice versa.

Field	Value	Description
		Default after power-up is Bit<0> = 0: FIFO connected to LVDS.
Bit 0	0	Connects FIFO to LVDS. Reset state.
	1	Connects the EMIFB registers goutA, goutB, goutC, foutD, foutE, foutF to LVDS.

Table 5.45: The Bypass Register Set (goutA - goutC, foutD - foutF)

Acronyms	Local Address	Function	Mode R/W	Bit
goutA	60000064	Bypass Register A	R/W	15−0
goutB	60000068	Bypass Register B	R/W	15−0
goutC	6000006C	Bypass Register C	R/W	15−0
foutD	60000098	Bypass Register D	W	15−0
foutE	6000009C	Bypass Register E	W	15−0
foutF	600000A0	Bypass Register F	W	15−0

Bypassing the FIFO and the Sequencer, the software on DSP can transmit the content of these pre-loaded registers via LVDS.

The transmit process is triggered by “dstrb” (see below).

The content of all registers can be read back and checked (see below).

Function	Condition	Description
Write to dstrb	semif = 1 selfg = 0	Transmitting the content of goutA, −B, −C and fout D, −E, −F as 2 words A and B in F−controller format for the SGU. The bits 46, 47, 48 are hardware controlled.
Write to dstrb	semif = 1 selfg = 1 goutA<1> = 1 goutA<0> = 0	Transmitting the content of goutA, −B, −C as 1 gradient data word in G−controller format.
Read from goutA, goutB, goutC	selgf = 0 semif = 1 srgs = 0	Provides the content of gout register A, B, C.
Read from goutA, goutB, goutC	selgf = 0 semif = 1 srgs = 1	Provides the content of fout register D, E, F.
Read from goutA, goutB, goutC	selgf = 0 semif = 0	Provides the content of the FIFO output.

Table 5.46: Bypass Registers goutA, goutB, goutC to LVDS as SGU-A-Word

LVDS Bit	48	47	46	45	44	43	42	...	33	32	...	17	16	...	1
gout	not applied			goutC 12...0						goutB 15...0			goutA 15...0		
Meaning on SGU	PAR	SYN	WID =0	PLS	PA	A	REG 9...0			PHASE 15...0			SHAPE 1...0		

Table 5.47: Bypass Registers foutD, foutE, foutF to LVDS as SGU-B-Word

Bit	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	...	17	16	...	1
fout	not applied			foutF 12...0													foutE15...0			foutD15...0		
Meaning on SGU	PAR	SYN	WID = 1	NCO_SEL 2...0			REG_VAL 1...0		F_VAL 2...0			PH_VAL 1...0		SH_VAL	F_DATA 33...0							

Table 5.48: Bypass Regs. goutA, goutB, goutC to LVDS, Gradient-Data-Word

Bit	48	47	...	44	43	...	38	37	...	33	32	.. .	18	17	16	...	6	5	4	3	2	1
gout	na	goutC 15...0									goutB 15...0				goutA 15...0							
Meaning on Gradient Amplifier	PAR	MSB Address							MSB Data					Data (res)			(res)			LAST	VALID	NG
		ADD<9...6>				ADD<59...0>			DATA<19...0>					gnd			gnd					

Table 5.49: Generate Data Valid Strobe (dstrb)

Acronyms	Local Address	Function	Mode R/W	Bit
dstrb	6000005C	Generate data valid strobe.	W	x

Writing to this address (no data) sends one or two words out of the gout-registers and fout registers respectively via the LVDS port (if the registers are selected, addr 60000058):

Function	Condition	Description
Write to dstrb	semif=1 selfg=0	Transmitting the content of goutA, −B, −C and foutD, −E, −F as 2 words A+B in F−controller format for the SGU. The bits 46, 47, 48 are hardware controlled.
Write to dstrb	semif=1 selfg=1 goutA<1>=1 goutA<0>=0	Transmitting the content of goutA, −B, −C as 1 Gradient data word in G−controller format.

Table 5.50: Generate Next Grad Signal (ngs)

Acronyms	Local Address	Function	Mode R/W	Bit
ngs	60000060	Generate next gradient signal.	W	x

Writing to this address (no data) sends one or two words out of the gout-registers and fout- registers respectively via the LVDS port (if the registers are selected, addr 60000058):

Table 5.51: Bypass Regs goutA, goutB, goutC to LVDS, Next Gradient Word

Bit	48	47	...	33	32	...	17	16	...	3	2	1
gout	na	goutC 15...0			goutB 15...0			goutA 15...2			n.a.	
Field	PAR				not allocated					!LAST	1	0

Function	Condition	Description
Write to nsg	semif=1 selfg=1	Transmitting the content of goutA, -B, -C as next gradient word in G-controller selfg=1 format.

Table 5.52: Select Register Set (srgs)

Acronyms	Local Address	Function	Mode R/W	Bit
srgs	600000A4	Select register set for read back.	W	0

This 1-bit register selects the register goutA, -B, -C or fout-D, -E, -F for reading back of its content, both via the addresses of the gout register 60000064, -68, -6C:

Field	Value	Description
		Default after power-up, sequencer reset “seqres” and reset is Bit<0> = 1: foutA, -B, -C selected.
Bit 0	0	Connects the outputs of the registers goutA, goutB, goutC to EMIFB 1.
	1	Connects the outputs of the registers foutD, foutE, foutF to EMIFB.

Table 5.53: LVDS Deskew Operation (lvds_dsk)

Acronyms	Local Address	Function	Mode R/W	Bit
lvds_dsk	600000A8	LVDS Deskew	R/W	1-0

The register is provided for controlling the deskew process of the LVDS transmitter. Deskew initiates sending a test sequence which enables the receiver to compensate the delay difference between the line pairs of the cable. To be successful, deskew needs also to be enabled at the receiver.

Deskew is not important if the cable is shorter than 3 meters.

Deskew is carried out after power-up and should also be carried out by a software command if the LVDS connection have been interrupted without subsequent power-up.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied														DSK_Flag	LVDS_DSK

Field	Value	Description
LVDS_DSK		R/W
	1	Deskew not active; normal data send mode; this is the state after reset or power-up.
	0	Deskew command; process active, sending test sequence.
DSK_Flag		R/-
	1	Deskew not yet carried out after last power-up or last line interrupt.
	0	Deskew have been carried out; state reached by LVDS_DSK=0.

Registers Used on T-Controller Only *5.7.7.3*

Register Description: RCP Output Register and Version Register on EMIFB, space CE0

Table 5.54: Read Board Version Register via TCTRL (t_brdv)

Acronyms	Local Address	Function	Mode R/W	Bit
t_brdv	6000003C	Board version of IPSO AQS ACQ	R	15-0

The revision number makes important hardware features identifiable.

So far valid for IPSO AQS ACQ only.

Bits	15		8	7		0
Fields	Board Rev			Sub-Rev		

Field	Value	Description
Board Rev		R/-
	00	IPSO 19“: Default. IPSO AQS: ACQ board with 5 controllers and 16 MByte RAM + TMS320C6415; H12549.
	02	IPSO AQS: ACQ board with 5 controllers and 128 MByte RAM + TMS320C6455; Hxxxxx.
Sub Rev		R/-
	00	IPSO 19“: Default. IPSO AQS: ACQ board with 5 controllers and 16 MByte RAM + TMS320C6415; H12549. ACQ board with 5 controllers and 128 MByte RAM + TMS320C6455; Hxxxxx.

Table 5.55: Disable/Enable RCP Outputs (rcpout)

Acronyms	Local Address	Function	Mode R/W	Bit
rcpout	60000028	Disable/enable RCP outputs.	-/W	0

1-bit register to enable or disable (high impedance state) the RCP outputs (Coax).

The RCP outputs are disabled after power-up or reset.

They are pulled to 5-volt.

This register has no function, if the TxCtrl is used as F-controller or G-controller.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied															rcpout

Table 5.56: Register rcpout

Field	Value	Description
rcpout		-/W
	0	RCP outputs active.
	1	RCP outputs inactive; State after reset, power-on and command rcpdis.

Table 5.57: RCP Output Register 0-4 (tout0-tout4)

Acronyms	Local Address	Function	Mode R/W	Bit
tout4	60000040	TCTRL Output Register 4	R/W	5−0
tout3	60000044	TCTRL Output Register 3	R/W	15−0
tout2	60000048	TCTRL Output Register 2	R/W	15−0
tout1	6000004C	TCTRL Output Register 1	R/W	15−0
tout0	60000050	TCTRL Output Register 0	R/W	15−0

Normally the RCP outputs are controlled by the bit stream of the FIFO output bits. Using register ”selrcp”, the RCP’s can be disconnected from the FIFO and connected to the RCP

Output Registers. This requires presetting the registers with the desired value. This can be done when the RCP’s are in high impedance state (after Power-up or if rcpout=1).

The register contents can be read back via their outputs if rcpout=1 (see below).

Table 5.58: Relations Between tout-Registers, FIFO-Words and setnmr-Words

Bit	15	...	6	5	4	3	2	1	0	15	...	0	15	...	0	15	...	0	15	...	0
Register	not applied			tout4						tout3			tout2			tout1			tout0		
FIFO Word	not applied			A (64...58)						B (64...2)											
setnmr	not applied						setnmr0 (34,33, 32)			setnmr4 (31...0)						setnmr3 (31...0)					
RCP out	not applied			69	68	67	66	65	64	63	...	48	47	...	32	31	...	16	15	...	0

Table 5.59: T-Controller Output Register tout0...tout4

Function	Condition	Description
Write to tout0...tout4	selrcp = 1	Setting the registers without any effect to the RCP outputs.
	rcpout = x	Switching the source of the RCP outputs from FIFO to tout0...4.
Read from tout0...tout4	rcpout = 1	Reading the contents of tout0...4.

Table 5.60: Select FIFO or RCP tout-Register (selrcp)

Acronyms	Local Address	Function	Mode R/W	Bit
selrcp	60000054	Select FIFO or tout-Registers as RCP source.	-/W	0

1-bit register to select the tout-Registers or the FIFO outputs to be the source for the RCP outputs (coax).

After changing the selection to the FIFO, the RCP outputs keep the contents of the tout registers up to the time when the Sequencer sends the next RCP data word out of the FIFO.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied															selrcp

Table 5.61: Register selrcp

Field	Value	Description
selrcp		-/W
	0	tout registers selected as RCP source.
	1	FIFO selected as RCP source; Default state after reset and power-On.

Read Version of Sequencer FPGA

Table 5.62: Read Version of Sequencer FPGA (fpgavsn)

Acronyms	Local Address	Function	Mode R/W	Bit
fpgavsn	6000002C	Read Version of Sequencer FPGA.	R/-	15-0

A read access of this address delivers the version of the Sequencer logic (Stratix FPGA). The default value is 0x0001.

Table 5.63: Sequencer Program Version

Field	Value	Description
fpgavsn	0001	Default or first shipped version.

Register Description: AQ-Bus Control Register on T-controller, EMIFB, sr_counter, space CE1

The following registers control the global AQ bus functions. These functions affect all controllers in the system.

These registers are exclusively accessible on the Tx-controller operating as T-controller.

Table 5.64: Start Sequencer (seqstart)

Acronyms	Local Address	Function	Mode R/W	Bit
seqstart	64000078	Start the sequencer.	-/W	xxxx

A write access to this address (without data) sets the Start Flag and consequently activates the AQSTART signal of the AQ-Bus which initiates all controllers to start.

Setting the Start Flag is synchronized with the 20 MHz clock and the Next-Value clock of the Gradient channel.

Table 5.65: Stop Sequencer Device Code (seqstop)

Acronyms	Local Address	Function	Mode R/W	Bit
seqstop	6400007C	Stop the sequencer.	-/W	xxxx

A write access to this address (without data) clears the Start Flag and consequently clears the AQSTART signal of the AQ-Bus which initiates all controllers to stop.

The partial sequencers of all controllers stop and interrupt their respective DSPs (DSP EXT_INT4).

Table 5.66: Clear AQSTART (aqst_clr)

Acronyms	Local Address	Function	Mode R/W	Bit
aqst_clr	64000074	Clear AQSTART (Sequencer Stop).	-/W	xxxx

Just like seqstop, a write access to this address (without data) clears the Start Flag and consequently clears the AQSTART signal of the AQ-bus which initiates all controllers to stop and to interrupt their respective DSPs (DSP EXT_INT4).

The aqst_clr is also carried out by power-up and reset.

Table 5.67: Control of AQSTART

Field	Value	Causal Event	Condition	Description
AQSTART	1 -> 0	Write to seqstart.	RUN	All partial Sequ. being in RUN mode, start working.
	0 -> 1	Write to seqstop.	-	All partial Sequ. stop and enter the IDLE state; Next RUN state not until Write to seqlst; DSP EXT_INT4 initiated.
	0 -> 1	Write to aqst_clr reset	-	All partial Sequ. stop and enter the IDLE state; Reset next RUN state not until Write to seqlst; DSP EXT_INT4 initiated; EXRDEN is set inactive

Table 5.68: Suspend Sequencer (seqsus)

Acronyms	Local Address	Function	Mode R/W	Bit
seqsus	64000080	Suspend of the sequencer.	-/W	xxxx

A write access to this address (without data) sets the SUSP_RES (suspend/resume) signal of the AQ-Bus to “1”. This causes two actions:

1. It initiates the sequencer of the “Master” channel to stop when the next suspend instruction occurs.
2. It sets the SUSPEND_WINDOW signal of the AQ-Bus to “1”.

Subsequently, every sequencer of a slave channel stops and enters the “suspend” state when it receives a instruction which is labeled as a “suspend instruction” from the FIFO. Necessary condition is SUSP_RES=1 and SUSPEND_WINDOW=1.

After power-up or reset (SEQRES) is SUSP_RES=1 (suspend state).

Table 5.69: Resume Sequencer (seqrsm)

Acronyms	Local Address	Function	Mode R/W	Bit
seqrsm	64000084	Resume of the sequencer.	-/W	xxxx

A write access to this address (without data) clears the SUSP_RES (suspend/resume) signal of the AQ-bus to “0”.

This causes the sequencer of all channels to count down their respective delay counters and resume reading instructions out of the FIFO. This operation starts simultaneously with a low-to-high slope of the 20 MHz clock and the Next Value clock.

Table 5.70: Control of Suspend/Resume

Field	Value	Causal Event	Condition	Description
SUSP_RES	0 -> 1	Write to seqsus reset.	suspend Instr.	Master sequencer stops and sets SUSPEND_WINDOW.
		Suspend Instr.	SUSP_RES=1 SUSPEND_WINDOW=1	Slave sequencers stop at next suspend instruction.
	1 -> 0	Write to seqrsm.	-	All sequencers resume their operation.

Table 5.71: Select Suspend Trigger (sustrig)

Acronyms	Local Address	Function	Mode R/W	Bit
sustrig	64000088	Trigger for suspend.	-/W	2-0

Writing data to this register selects an external trigger signal or the write access to seqsus and seqrsm as initiator for suspend/resume.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied													SUSP source		

Table 5.72: Register of Suspend Trigger Select

Field	Value	Description
SUSP Source	000	Write access to seqsus and seqrsm.
	001	External trigger Trig1.
	010	External trigger Trig2.

Table 5.72: Register of Suspend Trigger Select

	011	External trigger Trig3.
	100	External trigger Trig4.
	101	Write access to seqsus and seqrsm.
	110	Write access to seqsus and seqrsm.
	111	Write access to seqsus and seqrsm.

Table 5.73: Load Next-Value Counter (lgcnt)

Acronyms	Local Address	Function	Mode R/W	Bit
lgcnt	64000090	Load Next-Value counter.	-/W	15-0

Writing data to this register determines the time period “T” of the Next-Value clock (GCLK). This clock is generated by a 16-bit counter driven with 20 MHz.

Following, the time period T is adjustable between 100ns and 6,553ms and:

T = (n+1). 100ns

The default period after Power-up is 10 µs.

Together with the 20 MHz clock, the Next-Value clock is also used to synchronize AQSTART and SUSP_RES.

Table 5.74: Next-Value Counter

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	MSB							„n“								LSB

Table 5.75: Trigger signal synchronization (synctrig)

Acronyms	Local Address	Function	Mode R/W	Bit
synctrig	6400008C	Synchronize trigger with the Next-Value clock.	-/W	3-0

Writing data to this register selects the external trigger signals to become synchronized with the 20 MHz clock and the next value clock.

The trigger signal is selected by a “1” at its respective position.

Table 5.76: Next-Value Counter

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied												Trig4	Trig3	Trig2	Trig 1

Table 5.77: Emergency Stop Register (emstop)

Acronyms	Local Address	Function	Mode R/W	Bit
emstop	64000070	Synchronize trigger with the Next-Value clock.	-/W	3-0

Writing a “1” to bit0 of this register initiates the SGU_RES (SGU reset) signal and sets for the DSP of this channel the interrupt EXT_INT5 and the status signal SGURES_ST=0 (SGU reset status) at the global IO-pin GP8.

SGU_RES is a wired OR signal and can be activated by external devices too. In this case, SGURES_ST is set to “1” instead of “0”.

Table 5.78: Function of Emergency Stop

Field	Value	Causal Event	Condition	Description
SGURES	1 -> 0	Internal activated by write 0 to emstop.	-	SGURES=0 (active) SGURES_ST=0 (DSP Global IO-Pin GP8) DSP EXT_INT5 active
		External activated.	-	SGURES=0 (active) SGURES_ST=1 (DSP Global IO-Pin GP8) DSPEXT_INT5 active
	0 -> 1	Internal deactivated by write 1 to emstop, reset.	External not activated.	SGURES=1 SGURES_ST=1 (DSP Global IO-Pin GP8).

Synchronization of Pulse Program with the Spin Rotor Signal

This logic is implemented to support the software and the pulse program in dealing with the following tasks:

1. To ascertain the revolution speed of the spinner.
2. To count the number of turns.
3. To synchronize the pulse sequence with the rotation of the spinner and its position.
4. To stop the pulse sequence and restart it at the same position of the spinner after a predefined number of spinner turns have elapsed. The

position is measured as the number of 80 MHz clock cycles with respect to a trigger pulse representing the fixed zero-crossing of the spinner.

The logic uses two 32–bit counters (counter–1, counter–3), a 16 Bit counter 2, a read register and a signal called Trigger–A.

The logic provides the signals Trigger-B and Trigger-C.

Any external trigger signal out of Trig1...Trig4 has to be selected as Trigger -A, -B and -C.

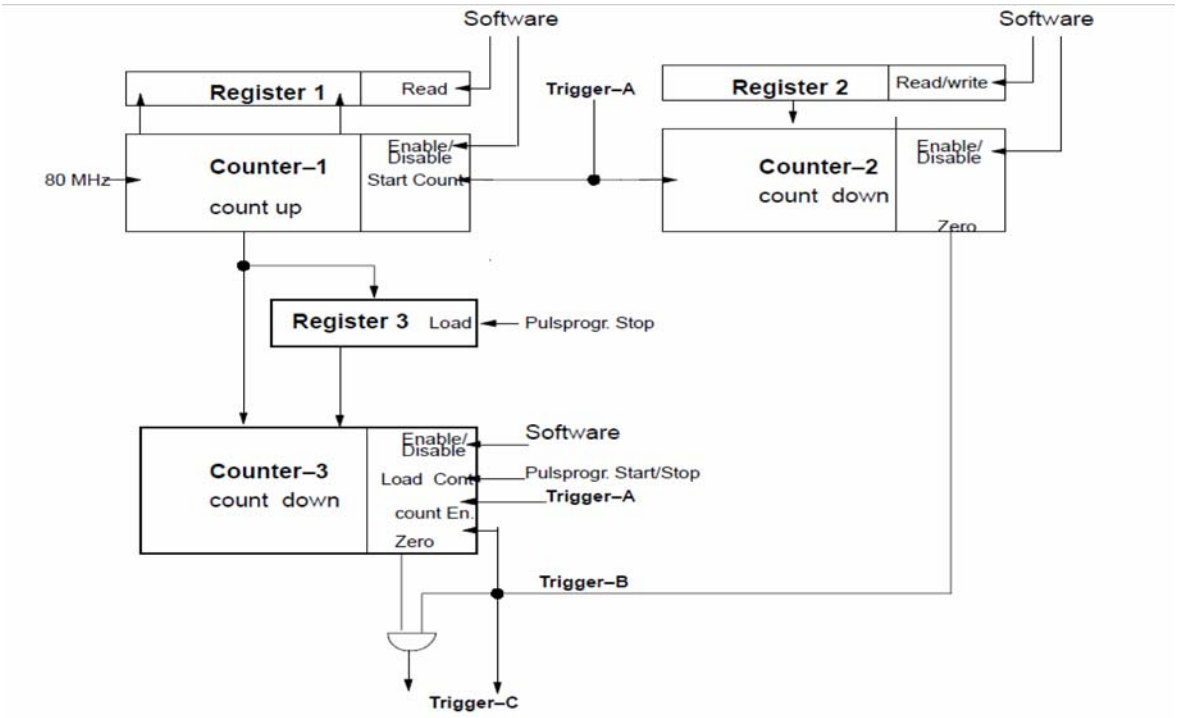


Figure 5.4: Counter Logic

Functional attributes of signals and recourses:

Trigger-A:	Pulse signal representing the zero-crossing of the spinner, selected out of Ext. Trigger 1...4.
Trigger-B:	Predefined number of spinner revolutions reached, internal used.
Trigger-C:	Predefined number of spinner revolutions and start position of next pulse sequence reached, internal used.
Counter–1:	32 bit counts 80 MHz clock cycles, forward between two zero–crossing (measureable period 25 ns – 53.6 sec).
Counter–2:	16 bit counts the predefined spinner revolutions, backward down to zero

Counter–3:	32 bit count down the time value, stored in register–3, between the Trigger A and the stop command if counter 2 has reached zero
Register-1, src1lo/src1hi:	32 bit holds and provides the value of counter–1 sampled at the last zero–crossing of the spinner (spinner rotation frequency).
Register-2, src2:	16 bit read/writeable by software; holds and provides the value for counter–2 to count the predefined spinner revolutions.
Register-3:	32 bit holds and provides the value of counter–1 sampled from the last Trigger A up to the stop command.

Table 5.79: Spin Rotation Trigger Select (srtrsel)

Acronyms	Local Address	Function	Mode R/W	Bit
srtrsel	640000AC	Spin rotation trigger select.	-/W	0-3

The assignment of the trigger signals Trig1,...,Trig4 to Trigger-A can be selected by a write to this register.

The setting of srtrsel0...srtrsel3 can be read back via the register “srcen”.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied												srtrsel 3-0			

Table 5.80: Select Reg. for External Trigger Source of Rotor Synchronisation

Field	Value	Description
SRTRSEL	X000	Ext. Trig1 -> SR Counter Trig. input.
	X001	Ext. Trig2 -> SR Counter Trig. input.
	X010	Ext. Trig3 -> SR Counter Trig. input.
	X011	Ext. Trig4 -> SR Counter Trig. input.
	X100	Ext. Trig1 -> SR Counter Trig. input; SR Counter Trig. output -> Int. Trig1.
	X101	Ext. Trig2 -> SR Counter Trig. input; SR Counter Trig. output -> Int. Trig2.
	X110	Ext. Trig3 -> SR Counter Trig. input; SR Counter Trig. output -> Int. Trig3.
	X111	Ext. Trig4 -> SR Counter Trig. input; SR Counter Trig. output -> Int. Trig4.

Table 5.80: Select Reg. for External Trigger Source of Rotor Synchronisation

	0XXX	Trigger-B (SR Counter2 Out) -> Int. Trigx
	1XXX	Trigger-C (SR Counter1 and Counter2 Out) -> Int. TrigX

Table 5.81: Spin Rotation Counter Enable (srcen)

Acronyms	Local Address	Function	Mode R/W	Bit
srcen	640000B0	Write srcen	-/W	0
		Read srcen	R	15-0

Setting Bit-0 of this register enables or disables the counters and the logic. After power-up, the state of Bit-0 is “0”, disabled and the counters are cleared.

Reading “srcen” gives back the states of the enable bit, the trigger select bits and the trigger status bits.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	not applied							synctrig 3-0				srtrsel 3-0				srcen

Table 5.82: Rotation Counter Enable

Field	Value	Cause of Event	Condition	Description
scren	0	Power-up	-	Disabled.
	0 -> 1	Write 1 to srcen	-	Enabled.
	1 -> 0	Write 0 to srcen	-	Disabled.

Table 5.83: Spin Rotation Counter-1 (register src1)

Acronyms	Local Address	Function	Mode R/W	Bit
src1lo	640000B4	Spin rotation counter 1 low word	-/R	15-0
src1hi	640000BC	Spin rotation counter 1 high word	-/R	15-0

Counter-1 increments with the 80 MHz clock and is cleared at each zero crossing of the spinner.

The register “src1lo and src1hi” represent a 32 bit value and will be updated with the content of Counter–1 at each zero–crossing of the spinner (src1lo = low word, src1hi = high word of counter1). Therefore, the content “N” of src1lo/src1hi are representing the revolution speed of the spinner :

The time for one revolution is: T = (N+1) x 12.5 nsec

T can be measured between Tmin = 25 nsec and Tmax = 53.6 sec

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
src1lo	MSB	src1lo: low word value of Counter-1 at previous zero-crossing.														LSB
src1hi	MSB	srchi: high word value of Counter-1 at previous zero-crossing.														LSB

Table 5.84: Rotation Counter-1

Field	Value	Cause of Event	Condition	Description
src1	0	Power-up	-	Disabled and cleared.
	0	srcen=1	Before stop.	Counter-1 is incrementing up to zero-crossing of the spinner.
	N	Zero-crossing	Before stop srcen=1	Content of counter posted to src1lo and src1hi; Counter-1 cleared and incrementing again up to zero-crossing of the spinner.
	N	Counter 2=0	After start srcen=1	Counter-3 decrements down to zero.
	N	Counter-3=0	After start srcen=1 Counter-2=0	Trigger-C restarts the pulse program.

Table 5.85: Spin Rotation Counter2 Register(src2)

Acronyms	Local Address	Function	Mode R/W	Bit
src2	640000B8	Read/write spin rotation counter 2.	W/R	15-0

Counter–2 decrements a preset value of spinner revolutions which it assumed from its preregister src2. The pulse program starts the Counter–2 and the counter–2 stops when it reaches zero. Counter–2 is reloaded with the content of the scr2 register on the next start command.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	MSB	src2: Value of Counter-2														LSB

Table 5.86: Rotation Counter-2

Field	Value	Causal Event	Condition	Description
src2	0	Power-up	-	Disabled and cleared.
	0	srcen=1	Before start.	Counter-2 set with content of src2
	R	Write to src2	Before start srcen=1	Counter-2 set to a number of spinner revolution's to be carried out after start from pulse program.
	R > r > 0	Start of Counter-2 from pulse program	After start srcen=1	Counter-2 decrements at each zero-crossing of the spinner.
	0	Counter-2=0	After start srcen=1	Counter-2 reaches zero and starts Counter-3 to count backwards.

Engineering Design 5.8

IPSO-Tx for the IPSO 19" model 5.8.1

Dimensions

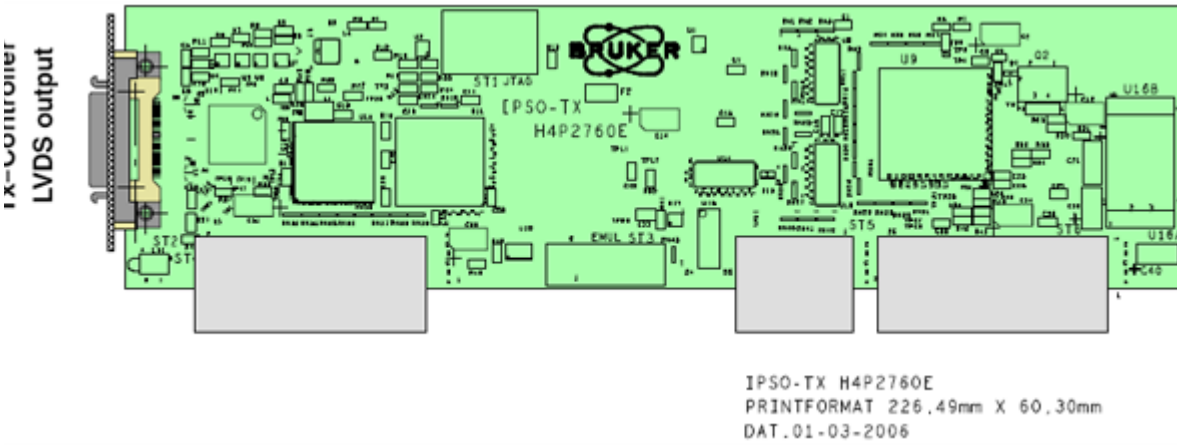


Figure 5.5: Tx-controller Board for the IPSO 19" Unit

Ports

Data Output

- Low voltage, low noise LVDS input via 8 balanced data lines and 1 clock line.

- Transfer rate of 80 mega-words per second (480 Mbyte/s).
- Word width 48 bit.

Power Requirements

Table 5.87: Power Requirements

Part Number	Assembly	+5 V	+3.3 V	+12 V	+5 VSB	-12 V
H12538F2	Tx-controller	0.6 A	0	0	0	0
H12538F3	Tx-controller	not available	0	0	0	0

The connector of this port is located at the solder (back) side of the PCB. So several adapters with different cable connectors can be mounted next to this board.

This port comprises the following signals:

JTAG Structure and BBIS-EEPROM *5.8.2*

For programming and testing during production, the Tx-controllers provide a JTAG interface to 3 JTAG chains. Furthermore, the application software reads the board information (type, version, serial number, EC level) via this interface.

The DSP can be accessed by an emulation software via a separate connector and the parallel port of a PC.

Another separate connector allows bypassing the bridge and the direct access of chain 3.

Table 5.88: JTAG Structure on IPSO Tx-controller Board of the IPSO 19” Unit

Connector	Stxxx			Stxxx		
JTAG Bridges	Uxx, Addr=0xX			U18, Addr=0x2		
Connector	–	ST??	ST??	–	ST??	ST??
JTAG Chain	Chain1	Chain2	Chain3	Chain1	Chain2	Chain3
Devices					U9:DSP	U3:EEPROM
						U12:FPGA
						U11:FIFO

Connector Pin Allocations 5.9

LVDS Connector

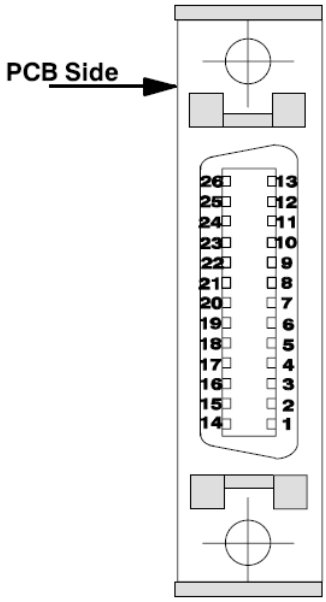


Figure 5.6: Pin Location of the 48-Bit LVDS Connector at the PCB

Table 5.89: LVDS Connector: Cable and Pin Assignment

Function	Type of Wire	Transmitter Signal	Receiver Signal	Pin No.
Signal: Differential pair of the received serial transmit clock connected to the corresponding inputs of the transmitter.	Twisted and shielded	TxCLK_P	RxCLK_P	6
		TxCLK_M	RxCLK_M	18
Shield: Common drain wire of all separate shields, connected to CHASSIS.		LVDS Gnd		26
Signal: Differential pair of the received serial data stream connected to the corresponding inputs of the transmitter.	Twisted and shielded	TxIN_P0	RxIN_P0	3
		TxIN_M0	RxIN_M0	15
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P1	RxIN_P1	4
		TxIN_M1	RxIN_M1	16
Shield.		LVDS Gnd		26

Table 5.89: LVDS Connector: Cable and Pin Assignment

Function	Type of Wire	Transmitter Signal	Receiver Signal	Pin No.
Signal.	Twisted and shielded	TxIN_P2	RxIN_P2	5
		TxIN_M2	RxIN_M2	17
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P3	RxIN_P3	9
		TxIN_M3	RxIN_M3	21
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P4	RxIN_P4	10
		TxIN_M4	RxIN_M4	22
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P5	RxIN_P5	11
		TxIN_M5	RxIN_M5	23
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P6	RxIN_P6	12
		TxIN_M6	RxIN_M6	24
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P7	RxIN_P7	13
		TxIN_M7	RxIN_M7	25
Shield.		LVDS Gnd		26
USB signal pair, left open	Twisted and shielded	USB+		1
		USB-		14
Shield of the USB signal pair, connected to the CHASSIS.		USB Gnd		2
Signal: Connected to bit-0 of the register „chanconf“ on F- and G-controller.	Individual	CHANNEL_DETECT0		7
Signal: Connected to bit-0 of the register „chanconf“ on F- and G-controller.	Individual	CHANNEL_DETECT1		20
VCC of USB power, left open.	Individual	USB pwr		19
GND of USB power, connected to GND.	Individual	USB gnd		8
Common shield of the entire bundle.	Shield	CHASSIS		body

CHASSIS 5.9.1

The chassis is a separate plane in the PCB layer stack. This plane is stacked close by the ground plane, giving a very tight capacitive (only capacitive) and low inductance coupling to GND. The chassis plane is screwed together with the external chassis along the front edge near the connectors and the line drivers.

This solution reduces the digital noise at that point and the noise which is picked up by the driver and carried to the outside. Additionally, this avoids parasitic current through the GND plane which could be caused by potential differences of the remote device.

DS_OPT, Deskew optimization

DS_OPT of the transmitter is triggered after power up and under software intervention.

At the receiver this pin should be configurable to High or Low which would enable or disable the receiver to optimize the skews.

Rx Controller

6

Versions

Location	Name	Part Number	Increments
IPSO 19”	IPSO Rx-Controller	H12532	
IPSO 19”	IPSO Rx-Controller	H12532F1	Flash
PCI Bus	PCI Rx-Controller	H12565	Flash

Features

- The Rx-controller is able to receive 48−bit words via its LVDS−Input at a clock rate of 80 MHz if connected to a Tx-controller and at a rate of 100 MHz if connected to a DRU−M.
- Rx measures the time distance of each Tx A−Word from the previous one and stores this value as a number of receive clock cycles in the upper 16−Bit of the 64−Bit receive FIFO word.
- Receive FIFO for 8K Words of 64 bit connected to the EMIFA bus of the DSP 64−bit DSP TMS320C6415 with 1 MByte on−chip RAM, EMIFA, EMIFB, SDRAM and PCI−32Bit/33Mhz, interface.
- External RAM of 2 MByte/16 MByte connected to the EMIFA bus.
- EMIFA data bandwidth of 160 MWords of 64 bits.
- Separate EMIFB bus for control functions.
- FLASH PROM for board and revision information.

Architecture

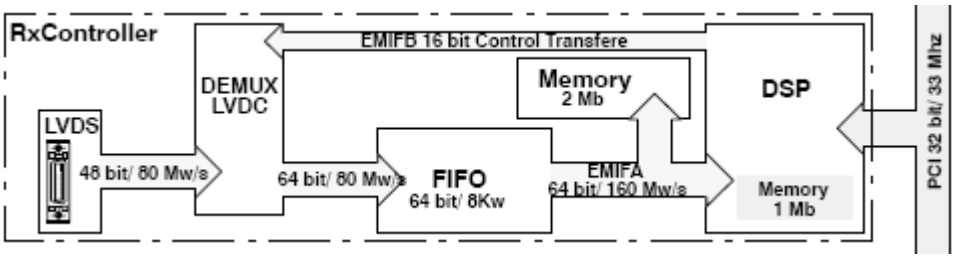


Figure 6.1: The Rx-Controller

Operation

The Rx-controller is designed to receive data words of 48−bits sent by the IPSO Tx-controller or the DRU.

These data words are received on 8 line pairs in a serialized form. They are transferred to parallel words in the LVDS receiver and delivered to the LVDC (FPGA) at a clock rate of 80 MHz (FCtrl, GCtrl) or 100 MHz (DRU). In the LVDC, the words are checked (validity and parity) and assigned with a time stamp fed into the FIFO. In case of a parity error, the parity flag in the status register is set and hold up to the FIFO will be cleared.

The 3 possible data sources (FCtrl, GCtrl, DRU) send in different formats. Therefore, 3 receiving modes have been implemented in the LVDC and selected depending on the recognized source.

The 48 bit words are stored in a FIFO which is 64 bit wide. The upper 16 bits of the FIFO words are used to hold the time stamps of each word. This time information gives the distance to the preceding word measured in numbers of clocks. The type of words which are measured and get the stamp depend on the receiving mode.

In the FCtrl mode the A−words are used. In the GCTRL mode the distance between two NG words is counted. In the DRU mode, the counting starts with each Control Word and ends at the following Control or Data Word.

The FIFO words can be processed by the DSP, transferred to its local memory or via the PCI bus.

The control and status register can be accessed by the DSP via the EMIFB bus. All registers and both memories of the Rx-controller can also be accessed by any other controller via the PCI Bus.

Structure of Input Words at the LVDS Receiver and the FIFO *6.1*

Dependent on the connected data source and the associated receiving mode, the Rx-controller checks the validity and the parity of the incoming words (A−, B-words in FCtrl mode; Gradient data and NG-words in GCtrl mode; Data− and Control words in DRU mode).

The resulting error status and the FIFO status can be read on the EMIFB bus.

Words from F−Controller *6.1.1*

A data package from the F−Controller consists of 2 Words (A+B) in adjacent clock cycles. The TIME value in the upper 16 bits of the FIFO word is the number of clock cycles between the previous A−Word and this one.

Table 6.1: F−Ctrl Words at Output of LVDS Receiver and FIFO (F−Ctrl Mode)

Bit		64	...	49	48	47	46	45	...	1
Word A	At LVDS	not used			PAR	SYNC	WID	Data from F−Controller		
Word B	At LVDS	not used			PAR	SYNC	WID	Data from F−Controller		
Word A	At FIFO	TIME value, low part			PAR	SYNC	WID	Data from F−Controller		
Word B	At FIFO	TIME value, high part			PAR	SYNC	WID	Data from F−Controller		

Table 6.2: Bit Fields of the F−Controller Output Word

Field	Value	Description
WORD_ID(WID)		Bit 46 in every word.
	0	Word A.
	1	Word B.
SYNC		Reflects the current state of the 20−MHz reference clock at transmitter.

Words from G−Controller *6.1.2*

A gradient switching package from the G−Controller consists of a variable number of gradient data words and 1 Next gradient word. Usually, these words are transmitted in adjacent clock cycles but this is not necessary.

The TIME value in the upper 16 bits of the FIFO word is the number of clock cycles between the previous Next gradient word and this one.

Table 6.3: G−Ctrl Words at Output of LVDS Receiver and FIFO (G−Ctrl Mode)

Bit		64	...	49	48	47	...	3	2	1
Next gradient	At LVDS	not applied			Parity	Not allocated			!VALID	!NG
Gradient data	At LVDS	not applied			Parity	Gradient			!VALID	!NG
Next gradient	FIFO	TIME value, low part			Parity	Not allocated			!VALID	!NG
Gradient data	FIFO	TIME value, high part			Parity	Gradient			!VALID	!NG

Table 6.4: Bit Fields of the G−Controller Output Word

Field	Value	Description
!VALID:!NG		These bits identify the gradient data words and the Next gradient words which activate the gradients transmitted since the previous Next gradient word.
	00	Not allowed, erroneous combination.
	01	Gradient data word.
	10	Next gradient word.
	11	Idle cycle without data.
PARITY		The even parity bit, created form bit 1 to 47.

Words from the DRU *6.1.3*

Table 6.5: DRU Words at Output of LVDS Receiver and FIFO (DRU Mode)

Bit		63	...	48	47	46	...	2	1	0
DRU Control Word	At LVDS	Not applied			Parity	DRU Control Information			1	0
DRU Data Word	At LVDS	Not applied			Parity	DRU Data			0	1
DRU Control Word	At FIFO	Time value, low part			Parity	DRU Control Information			1	0
DRU Data Word	At FIFO	Time value, high part			Parity	DRU Data			0	1

Table 6.6: Bit Fields of the DRU−Controller Output Word

Field	Value	Description
!Data...!CTRL		These bits identify the DRU data words and the control words (data and header/ trailer information)
	00	Not allowed, erroneous combination.
	01	Data word.
	10	Control word.

Table 6.6: Bit Fields of the DRU−Controller Output Word

	11	Idle cycle without data.
PARITY		The even parity bit, created form Bit 1 to 47.

Software Interface 6.2

Nearly all resources of the Rx-controller can be accessed by both, software running local or software running on the Host Controller. Only the FIFO is excluded from this. The FIFO can be accessed by the DSP only.

Both address ranges, local DSP and global PCI bus, are defined by 32 bit addresses. The access from the PCI range into many local ranges is possible through address windows, 2 ones dedicated to each controller. This is a 4 MByte window (for prefetchable accesses) and a 8 MByte window (for nonprefetchable accesses). The segmentation of the PCI address range to the window spaces the controllers is carried out by the BIOS and fixed by defining the content of all PCI base registers.

Every window can be moved through the local address range by modifying the content of the DSP page register (DSPP).

PCI Addresses 6.2.1

The content of the Base0 register is defined by the BIOS of the host controller.

The content of the DSPP register can be written by the software running on the host controller. This register can be reached through the nonprefetchable window.

Table 6.7: Relations Between PCI− and Local Addresses on R−Controller

	4 MByte Prefetchable Range		**8 MByte Nonprefetchable Range**	
	Bit [31...22]	Bit [21...0]	Bit [31...23]	Bit [2...0]
PCI Address	<Base0>	AD [21...0]	<Base1>	AD [22...0]
Local Address	<DSPP>		0000 0001 1	

Local Address Layout *6.2.2*

Table 6.8: Memory Map of the DSP 6415 on R-Controller

Local Hex Address Range	Block Size (Bytes)	Bus	Data Bus Width (Bytes)	Description	Utilization
000x xxxx	1M	Internal	8	On chip RAM	
0180 0000 − 0183 FFFF	256K	Internal		EMIFA config. register	
0184 0000 − 0187 FFFF	256K	Internal		L2 Cache config. register	
0194 0000 − 0197 FFFF	256K			Timer 0 register	
0198 0000 − 019B FFFF	256K			Timer 1 register	
019C 0000 − 019F FFFF	256K			Interrupt select register	
01A0 0000 − 01A3 FFFF	256K			Enhanced DMA register	
01A8 0000 − 01AB FFFF	256K	Internal		EMIFB config. register	
01AC 0000 − 01AF FFFF	256K	Internal		Timer 2 register	
01B0 0000 − 01B3 FFFF	256K	Internal		GPIO register	
01C0 0000 − 01C3FFFF	256K			PCI Register	
6000 0000 − 63FF FFFF	64M	EMIFB CE0	2	External RAM	Register
6400 0000 − 67FF FFFF	64M	EMIFB CE	2	External RAM	
6800 0000 − 6BFF FFFF	64M	EMIFB CE2	2	External RAM	BIS Flash Prom
6C00 0000 − 6FFF FFFF	64M	EMIFB CE3	2	External RAM	
8xxx xxxx	256M	EMIFB CE0	8	External RAM	
9xxx xxxx	256M	EMIFB CE	8	External RAM	
Axxx xxxx	256M	EMIFB CE2	8	External RAM	
Bxxx xxxx	256M	EMIFB CE3	8	External RAM	FIFO 16Kx64

Content of the DSP Configuration Registers 6.2.3

Table 6.9: EMIFA Configuration Register

Local Hex Address	Acronym	Value	Description
1800048	CE0SEC	00000042	EMIFA CE0 Space Secondary Control
1800044	CE1SEC	Unmodified	EMIFA CE1 Space Secondary Control
1800050	CE2SEC	Unmodified	EMIFA CE2 Space Secondary Control
1800054	CE3SEC	00000040	EMIFA CE3 Space Secondary Control
1800000	GBLCTL		EMIFA global Control
		00012724	Rx-controller with 2 MByte SRAM
1800008	CE0CTL		EMIFA CE0 Space Control
		FFFFFFE3	Rx-controller with 2 MByte SRAM
1800004	CE1CTL	Unmodified	EMIFA CE1 Space Control, not used
1800010	CE2CTL	Unmodified	EMIFA CE2 Space Control, not used
1800014	CE3CTL	FFFFFFE3	EMIFA CE3 Space Control, FIFO
1800018	SDCTL		EMIFA SDRAM Control
		0248f000	Rx-controller with 2 MByte SRAM
180001C	SDTIM		EMIFA SDRAM Refresh Control
		003F05DC	Rx-controller with 2 MByte SRAM
1800020	SDEXT		EMIFA SDRAM Extension
		00175F3F	Rx-controller with 2 MByte SRAM

Table 6.10: EMIFB Configuration Register

Local Hex Address	Acronym	Value	Description
1A80000	GLBCTL	00012324	EMIFB global control.
1A80008	CE0CTL	5055C11D	EMIFB CE0 space control, register.
1A80004	CE1CTL	FFFFFFBF	EMIFB CE1 space control, not used.
1A80010	CE2CTL	2A22E80A	EMIFB CE2 space control, BIS flash prom.
1A80014	CE3CTL	FFFFFFBF	EMIFB CE3 space control, not used.

Table 6.11: GPIO Configuration Register

Local Hex Address	Acronym	Value	Use	Description
01B00000	GPEN	0x1FF		GPIO Bit Enable; Usage of the GPIO pins GP0...GP8 as IO pins.
01B00004	GPDIR	0xE	Not applied not applied not applied.	Direction of GPIO Pins adjusted as:
		-	Not applied.	GP0 Output.
		-	Not applied.	GP1 Output.
		-	Not applied.	GP2 Output.
		-	MCBSP2 enable of serial PCI Config Prom.	GP3 Output.
		-	Not applied.	GP4 Input.
		-	Not applied.	GP5 Input.
		1	FIFO full.	GP6 Input, EXT_INT6 of the DSP.
		0	FIFO not full.	GP6 Input, EXT_INT6 of the DSP.
		-	Not applied.	GP7 Input.
		-	Not applied.	GP8 Input.

Memory at EMIFA, Space CE0 *6.2.4*

The external RAM of the DSP has a word width of 64 bit. It is connected to the DSP via the EMIFA bus with a band width of 160 MWords per second.

Table 6.12: Type of External Memory used on the Rx-Controllers

Local Hex Address	Size [MByte]	Word [Byte]	Type	Bandwidth [MByte/s]	Type of Controller	Identification
8000 0000 – 801F FFFF	2	8 Byte	SRAM	1280	RCtrl H12532	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX
					RCtrl embedded in AQS host H12547	imbf=0001

FIFO at EMIFA, Space CE3 *6.2.5*

The FIFO (IDT72V3670) can store 8−KWords of 64 bits each. The multiplex logic LVDC fills the FIFO and the DSP reads the words out via EMIFA with a band width of 160 MWords per second.

Every FIFO word includes the received data of 48 bits and a time stamp of 16 bits.

Table 6.13: Type of FIFOs used on the Rx-Controllers

Local Hex Address	Size [KByte]	Word [Byte]	Type	Bandwidth [MBytes]	Type of Controller	Identification
B000 0000 − B00F FFF8	128	8 Byte	IDT72V3670	1280	RCtrl H12532	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX
					RCtrl embedded in AQS host H1254	imbf=0001

Flash Prom at the EMIFB Bus, Space CE2 *6.2.6*

Access features to the BIS Flash Prom:

Bus width: 2 Byte, Data bit 7...0 implemented, Data bit 15...8 not implemented; therefore this doubles the occupied address room.

Control of access: Number of clock cycles

Duration of access: Circa 85 nsec for write and 270 nsec for read access.

Table 6.14: Type of Flash Proms used on the Rx-Controllers

Local Hex Address	Size [KByte]	Word [Byte]	Type	Type of Controller	Identification
6800 0000 − 6801 FFFF	64	1 Byte		RCtrl H12532	imbf=FFFF or 0000 and slot_brdv=XFXX or X0XX
Flash Prom is part of AQS host H12547 and not connected to DSP of RCtrl	64	1 Byte		RCtrl embed. in AQS Host H12547	imbf=0001

Registers at the EMIFB Bus, Space CE0 *6.2.7*

All registers are accessed via the EMIFB bus.

Access features to the registers:

Bus width: 2 Byte, Data bit 15...0 implemented.

Control of access: Ready Controlled.

Duration of access: Circa 144 nsec for write and 120 nsec for read access.

Address Layout

Table 6.15: Device Codes on EMIFB (CEO Space), Existent on RCtrl

Register	Local Address	Function	Mode R/W	Bits
ctrl	60000000	Control Register	W	1, 0
fifores	60000004	FIFO Reset	W	-
sts	60000008	Status Register	R	15-0
channel	6000000A	Channel Register	R/W	3-0
chanconf	60000030	Channel Configuration	R	15-0
a lot_brdv	60000038	Slot and board version	R	15-0

Every read access to other addresses of the EMIFB bus than presented in this table delivers the content of the Status Register (sts).

Register Description

Table 6.16: Control Register (ctrl)

Register	Local Address	Function	Mode R/W	Bits
ctrl	60000000	Control Register	W	0

The receiving mode can be set by modifying these two bits.

A read of the status register (sts) delivers the current selection.

Bits	15		2	1	0
Fields	not applied			mod1	mod0
Reset State				0	1

Table 6.17: Control Register

Field	Value	Description
mod(1...0)		Modus of operation.
	X1	RCtrl connected to a F−Controller.
	00	RCtrl connected to a G−Controller.
	10	RCtrl connected to a DRU.

FIFO Reset (fifores)

Table 6.18: FIFO Reset (fifores)

Register	Local Address	Function	Mode R/W	Bits
fifores	60000004	FIFO Reset	W	-

Writing to this register without data resets counters and flags of the FIFO and resulting in a clear of the content.

The FIFO is also cleared by Power−up and a PCI−Reset.

Channel Register (channel)

Table 6.19: Channel Register (channel)

Register	Local Address	Function	Mode R/W	Bits
channel	6000000A	Channel register	R/W	3-0

The channel number of the Fx-Controller to which the software wants the RCtrl to be connected to is written (by the software) into this register.

The content of this register is shown at the front display. This is advantageous in test applications with multiple Rx-controllers.

The register is implemented in version = 2 and so on (seen in chanconf).

Bits	15		4	3	2	1	0
Fields	not applied			chan			
Reset State				0	0	0	1

Table 6.20: Control Register

Field	Value	Description
mod(3...0)	0000	Reset state.
	0001	Connect Rx-controller to a Fx-controller out of nine.
	...	
	1001	

Channel Configuration Register (chanconf)

Table 6.21: Channel Configuration Register (chanconf)

Register	Local Address	Function	Mode R/W	Bits
chanconf	60000030	Channel Configuration	R	15-0

The bits of the channel configuration register provide information about versions, functions and options.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	Board function			Version						FCTRL channel			External config. bit			

Table 6.22: Channel Configuration Register

Field	Value	Description
External Config. Bit (3...0)		“Board Function” specific meaning:
		On Rx-controller:
	1111	IPSO Rx-controller, H12532 PCI.
	1110	Rx-controller, H12565.
FCtrl Channel (6…5)		Indicates the FCtrl channel from 1 to 8. On TCTRL, GCtrl and RCtrl is FCtrl channel = 0.
	111	F-Controller 1
	110	F-Controller 2
	101	F-Controller 3
	100	F-Controller 4
	011	F-Controller 5
	010	F-Controller 6
	001	F-Controller 7
	000	F-Controller 8 or TCTRL GCtrl, RCtrl
Version (12…7)		“Board Function” specific meaning:
		On Rx-controller: Version of the “LVDC” FPGA.
	000001	LVDC version 1 on IPSO Rx-controller (H12532), without BIS Flash Prom and without Channel Register.
	000010	LVDC version 2 on the Rx-controllers with Flash and Channel Register and existent as IPSO− (H12532F1) and PCI Rx-controller (H12565).
Board Function (15…13)		Indicates the function of the channel.
	000	TCtrl
	001	FCtrl
	010	GCtrl
	100	RCtrl

Slot Board Vers. Register (slot_brdv)

Table 6.23: Slot−Board Vers. Register (slot_brdv)

Register	Local Address	Function	Mode R/W	Bits
slot_brdv	60000038	PCI slot and board version of a Tx-controller.	R	15-0

This register contains the slot address in the IPSO 19” unit and the hardware version.

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fields	Slot address				Board revision				Board sub-revision							

Table 6.24: Slot Board Version Register

Field	Value	Description
Board Revision		4−bit number of the RCtrl board version.
(11...8)	0000	IPSO Rx-Controller with 2 MB external RAM.
	0001	IPSO Rx-controller with 2 MB external RAM and Flash.
	0010	IPSO Rx-controller with 16 MB external RAM and Flash.
Board Sub-revision		Identification of any sub-revision.
(7...0)	00000000	
Field Slot Add	Value	Description slot address, relevant in the “IPSO 19” unit”.
(15...12)	0001	Slot 15
	0010	Slot 2
	0011	Slot 3
	0100	Slot 4
	0101	Slot 5
	0110	Slot 6
	0111	Slot 7
	1000	Slot 8
	1001	Slot 9
	1111	Default at the Rx-controller embedded in IPSO AQS Host, H12547.
	1011	Default at the PCI Rx-controller, H1256.

Status Register (sts)

Table 6.25: Status Register (sts)

Register	Local Address	Function	Mode R/W	Bits
sts	60000008	Status Register	R	7-0

The status register is read only. It contains the FIFO flags, the mode control bits and the transfer error bits. The register enters its reset state after power-up, reset and a write to the **fifores** address.

Bits	15	...	9	8	7	6	5	4	3	2	1	0
Fields	not applied			WERR	IR	PAF	OR	PAE	HFL	mod1	mod0	PERR
Reset State												

Table 6.26: Status Register

Field	Value	Description
WERR		Word error.
	1	A sequence or control bit error occurred since last FIFO reset. The cause depends on the selected mode.
IR		FIFO input ready, connected to EXT_INT6 of the DSP.
	0	Input ready, FIFO not full.
	1	FIFO full.
PAF		PAF, Flag of FIFO almost full; threshold adjusted to 32 words.
	0	The FIFO can accept less than 32 further words.
	1	The FIFO can accept at least 32 further words.
OR		FIFO output ready.
	0	Output ready to be read, FIFO contains at least one word.
	1	FIFO empty.
PAE		PAE, flag of FIFO almost empty; threshold adjusted to 32 words.
	0	FIFO contains less than 33 words.
	1	FIFO contains more than 32 words.
HFL		FIFO Half Full Flag.
	0	FIFO contains more than 4096 words.

Table 6.26: Status Register

	1	FIFO contains less than 4096 words.
mod(1...0)		Mode of operation.
	11	Reserved.
	10	F−Controller Mode: RCtrl connected to a F−Controller.
	00	G−Controller Mode: RCtrl connected to a G−Controller.
	01	DRU Mode: RCtrl connected to a DRU.
PERR		Parity Error of an input word.
	1	Error since last FIFO reset.

Data Acquisition and Time Measurement *6.3*

Data Acquisition

The receiving speed is 80−MWords per second from the Fx-Controller and 100 MWords per second from the DRU.

Every received data word is checked for:

- Being an empty or a valid data word, resulting in acceptance or rejection;
- Having the correct and expected position in the sequence, result is WERR of sts;
- Having the correct parity, result is PERR of sts.

Sequence violations or parity errors set the error flags but do not avoid storing the word in the FIFO. This is to provide a complete image of the defective sequence. The error flags are reset at Power−up, PCI−Reset or a write access to fifores.

Time Measurement

Every received word sequence consists of data−words and controlling key−words and idle or empty words. The stored sequence image (in the FIFO) includes only the key−words and their affiliated following data words of different number. There are no gaps.

Here, measurement of time means, counting the time distance of each keyword from the previous one as number of receiving clock cycles.

Keywords are:

- A-words of the sequence from the F−Controller

- NG-words of the sequence from the G−Controller
- Ctrl-words of the sequence from the DRU.

Setting the receiving mode in the control register selects the right key−words.

The time distance is measured by a 32−bit counter. The low part of the 32−bit value will be stored together with the key−word in the empty upper 16 bits of the 64−bit FIFO. Except for stream from the DRU, the upper part of the 32−bit value will be stored together with the next data word.

The word stream from the DRU provides no possibility to store the upper part of the counter. Therefore, the measurable time capacity is reduced to a 16−bit count.

With receiving the keyword, the counter is cleared and starts counting again at zero.

The maximum measurable time distance is:

- 53,687 seconds @ 80 MHz, Fx-controller.
- 655,36 microseconds @ 100 MHz, DRU.

R−Ctrl Operating in F−Controller Mode *6.3.1*

All A−words and the one B-words which follows an A-word in the next clock period will be stored. All A-words get a time stamp.

Table 6.27: Effect of Word ID in F-Controller Mode

Identifier	Value	Accepted	WERR	Sequential Situation	Time Measuring
WID	0	yes	-	A−word following a B−word.	Low part of timer inserted in this A−word and timer cleared.
	1	no	-	B−word following an A−word.	High part of timer inserted in this B−word.
	0	yes	0->1	A-word following an A-word.	Low part of timer inserted in this A−word and timer cleared.
	1	no	-	B-word following a B-word.	Counting.

R−Ctrl Operating in G−Controller Mode *6.3.2*

All NG−words (Next Gradient) and all Valid−words (gradient data words) will be stored. There are no constraints regarding, succession, number or clock period.

Every NG−word gets a time stamp measured from the preceding NG−word.

Table 6.28: Effect of Valid and NG Bit in G-Controller Mode

Identifier	Value	Accepted	WERR	Sequential Situation	Time Measuring
!Valid...!NG	00	yes	0->1	Undefined	Low part of timer inserted in this NG−word and timer cleared.
	01	yes	-	First valid-word following a NG-word	High part of timer inserted in this valid−word.
	01	yes	-	Valid-word after first valid-word following a NG-word.	Counting.
	10	yes	-	NG-word following an NG-word.	Low part of timer inserted in this NG−word and timer cleared.
	10	yes	-	NG-word following an NG-word.	Low part of timer inserted in this NG−word and timer cleared.
	11	no	-	Idle.	Counting.

R−Ctrl operating in DRU Mode *6.3.3*

All control words (!Ctrl=0) and all data words (!Data=0) will be stored.

There are streams of control words and, separated by idle words, back−to−back streams of data words. Every control word gets a time stamp measured from the preceding control word. Every data word gets a time stamp measured from the last preceding control word.

Table 6.29: Effect of Valid and NG Bit in G-Controller Mode

Identifier	Value	Accepted	WERR	Sequential Situation	Time Measuring
!Valid...!NG	00	yes	0->1	Undefined.	Low part of timer inserted in this word and timer cleared.
	01	yes	-	Data-word.	High part of timer inserted in this data−word, not cleared.
	10	yes	-	Ctrl-word.	Low part of timer inserted in this Ctrl−word and timer cleared.
	11	no	-	Idle.	Counting.

Form

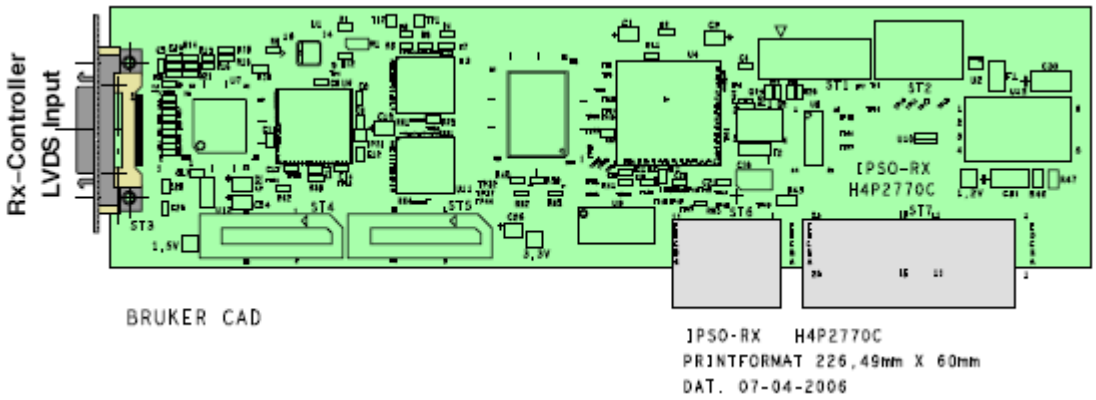


Figure 6.2: Rx-Controller of IPSO 19” Unit

Ports

Data Input

- Low voltage, low noise LVDS input via 8 balanced data lines and one clock line.
- Transfer rate 80 to 100 million words per second.
- Word width 48 bit.

JTAG Structure

The implemented JTAG interface has 3 chains. JTAG is used to program the logic, read the BIS Prom and debug the DSP operation.

Table 6.30: JTAG Structure on Rx-Controller of the IPSO 19”−Unit

Connector	Stxxx		
JTAG Bridge	Uxx, Addr=yy		
Connector	-	ST??	ST??
JTAG Chain	**Chain1**	**Chain2**	**Chain3**
		Uxx: DSP	Uxx: FIFO1
			Uxx: FIFO2

Table 6.30: JTAG Structure on Rx-Controller of the IPSO 19”−Unit

			Uxx: FIFO3
			Uxx: EEPROM (FPGA)

Power Requirements

Table 6.31: Currents

Part Number	Assembly	+5 V	+3.3 V	+12 V	+5 VSB	-12 V
H12532xx	Rx-controller	0.6 A	0	0	0	0

Pin Allocation of Connectors *6.5*

LVDS Input Connector

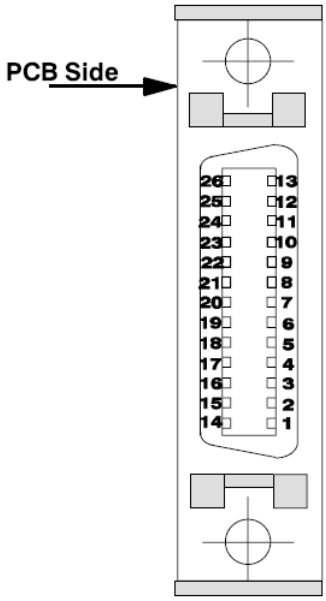


Figure 6.3: Pin location of the 48−Bit LVDS Connector at PCB

Table 6.32: LVDS Connector: Cable and Pin Assignment

Function	Type of Wire	Transmitter Signal	Receiver Signal	Pin No.
Signal: Differential pair of the received serial transmit clock connected to the corresponding inputs of the transmitter.	Twisted and shielded	TxCLK_P	RxCLK_P	6
		TxCLK_M	RxCLK_M	18
Shield: Common drain wire of all separate shields, connected to CHASSIS.		LVDS Gnd		26
Signal: Differential pair of the received serial data stream connected to the corresponding inputs of the transmitter.	Twisted and shielded	TxIN_P0	RxIN_P0	3
		TxIN_M0	RxIN_M0	15
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P1	RxIN_P1	4
		TxIN_M1	RxIN_M1	16
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P2	RxIN_P2	5
		TxIN_M2	RxIN_M2	17
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P3	RxIN_P3	9
		TxIN_M3	RxIN_M3	21
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P4	RxIN_P4	10
		TxIN_M4	RxIN_M4	22
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P5	RxIN_P5	11
		TxIN_M5	RxIN_M5	23
Shield.		LVDS Gnd		26
Signal.	Twisted and shielded	TxIN_P6	RxIN_P6	12
		TxIN_M6	RxIN_M6	24
Shield.		LVDS Gnd		26

Table 6.32: LVDS Connector: Cable and Pin Assignment

Function	Type of Wire	Transmitter Signal	Receiver Signal	Pin No.
Signal.	Twisted and shielded	TxIN_P7	RxIN_P7	13
		TxIN_M7	RxIN_M7	25
Shield.		LVDS Gnd		26
USB signal pair, left open	Twisted and shielded	USB+		1
		USB-		14
Shield of the USB signal pair, connected to the CHASSIS.		USB Gnd		2
Signal: Connected to bit-0 of the register „chanconf“ on F- and G-controller.	Individual	CHANNEL_DETECT0		7
Signal: Connected to bit-0 of the register „chanconf“ on F- and G-controller.	Individual	CHANNEL_DETECT1		20
VCC of USB power, left open.	Individual	USB pwr		19
GND of USB power, connected to GND.	Individual	USB gnd		8
Common shield of the entire bundle.	Shield	CHASSIS		body

Chassis

Chassis is a separate plane in the PCB layer stack. This plane is stacked close by the ground plane, giving a very tight capacitive (only capacitive) and low inductance coupling to GND. The chassis plane is screwed together with the external chassis along the front edge near the connectors and the line drivers.

This solution reduces the digital noise at that point and the noise which is picked up by the driver and carried to the outside. In addition this avoids parasitic current through the GND plane which could be caused by potential differences of the remote device.

DS_OPT, Deskew Optimization

DS_OPT of the transmitter is triggered after power up and under software intervention. At the receiver this pin should be configurable to High or Low which would enable or disable the receiver to optimize the skews.

Figures

Tables

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