



Bruker BioSpin

# Digital Preemphasis Processor ●

DPP1  
Technical Manual

Version 001

think forward

NMR Spectroscopy

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# Introduction

# 1

## Scope of this Manual

1.1

The DPP1 (Digital Pre-emphasis Board 1) is a Customer Replaceable Unit (CRU) used with Bruker AQS/3 type spectrometers with IPSO. This manual is intended for trained service and technical personnel and includes instructions on the installation and handling of the DPP1, as well as other detailed technical specifications and information.

The DPP1, is a standard PCI expansion card. It modifies the data stream sent by the gradient controller (G-Controller) to the gradient amplifier. The DPP1 is supervised by a software driver running under LINUX and has to be mounted in an PCI environment (see ***"Installation and Handling" on page 9***).

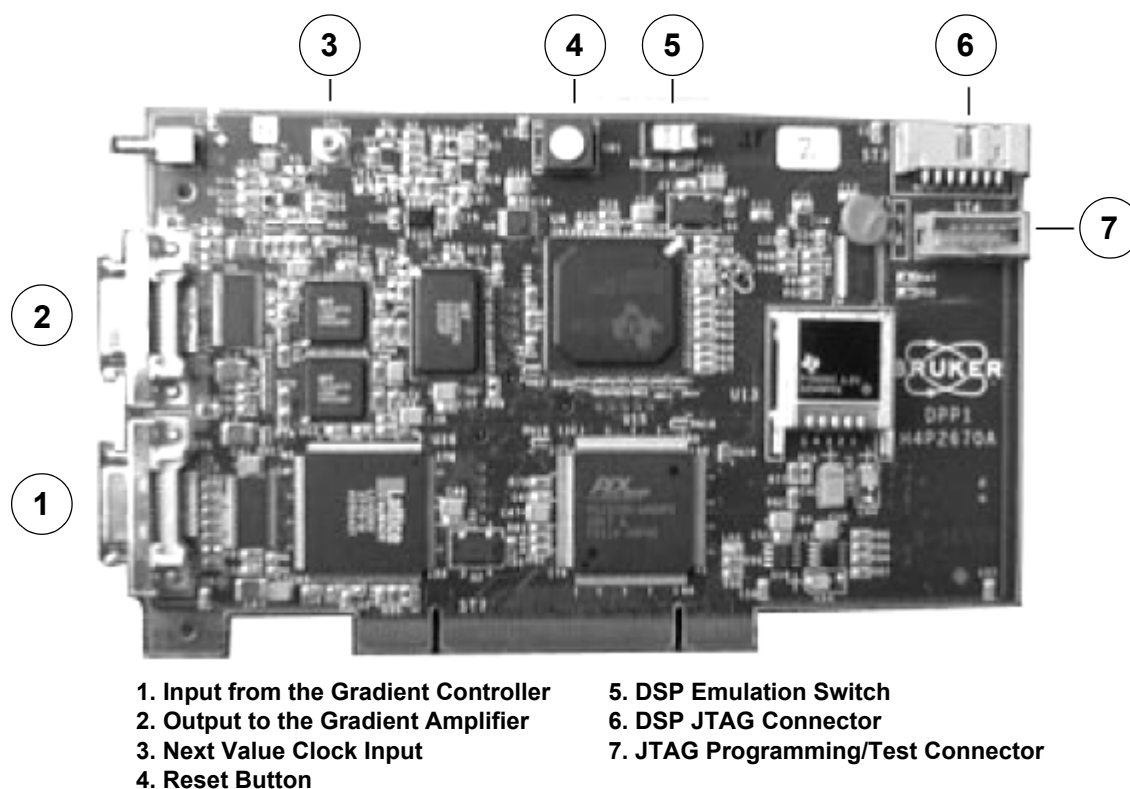


Figure 1.1. Top View of the DPP1

The DPP1 should only be used for its intended purpose as described in this manual. Use of the DPP1 for any purpose other than that for which it is intended is taken only at the users own risk and invalidates any and all manufacturer warranties.

Read this manual and pay particular attention to any safety related information before working with the DPP1.

These instructions refer to **all IPSO models**.

The IPSO may be damaged by inappropriate usage. The damage could be such, that the equipment must not be used before having been checked by a service representative.

The user should recheck the equipment at regular intervals for any damage or wear and is expected to inform the service representative immediately of any abnormality.



#### WARNING!

If you are in doubt about the correct state of any component, do not use the equipment and inform the service staff.

In the unlikely case of one of the following, stop using the equipment, disconnect the power supply, report the circumstance to the service staff and ask for instructions:

- The power cord, power plug or power supply are cracked, brittle or damaged.
- Signs of excessive heat are apparent.
- There is evidence or suspicion that a liquid has intruded into any enclosure.
- The power cord or the power supply have been in contact with any liquid.
- The IPSO has been dropped or damaged in any way.
- The equipment does not work correctly.



#### WARNING!

Do not try to service the equipment by yourself, unless you are specifically asked to do so and are given instructions by the service staff. In case of questions or problems, please contact your nearest Bruker office or representative.

**Special Safety Symbols**

1.3.1

These symbols are used on the equipment and/or throughout this manual. They alert to danger and important information:

There are various information notices used in this manual. These notices highlight important information or warn the user of a potentially dangerous situation.

**WARNING!**

This symbol denotes hints or instructions throughout this manual whose non-compliance could lead to erroneous or incalculable behavior of the system.

**WARNING!**

The symbol indicates a potential risk of injury due to contact with high voltage.

**Intended Use**

1.4

The DPP1 is to be used only in a PCI environment and with Bruker AVANCE III spectrometers for the modification of data streams sent by the gradient controller.

The board is not intended for use outside of these standard parameters.

**Contact for Technical Assistance**

1.5

For further technical assistance on the DPP1, please do not hesitate to contact your nearest BRUKER dealer or contact us directly at:

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# Installation and Handling

# 2

## Product Requirements and Handling

2.1

The DPP1 Digital Preemphasis Board is a Customer Replaceable Unit (CRU). To insert or remove the DPP1 follow the instructions in this manual.

Replacing CRU's requires opening of the enclosure. Before doing this, the unit must be completely switched off and unplugged or disconnected and dismantled from its rack.

## PCI Requirements

2.1.1

Type of PCI Bus:	32 bit/ 33 MHz
Length of the card:	Short, 176mm
PCI functions:	Single
Number of interrupts:	One at interrupt A, pin A6
PCI signal voltage:	The DPP1 can be used in 3.3 V or 5 V buses.

Signals received have to be between 3.3 V to 5 V (5 V tolerance).

The level of signals sent depends on the voltage at the "V<sub>I/O</sub>" pins A16, B19, A59 and B59 of the PCI slot used.

## Handling

2.2



Handling under ESD safety conditions is necessary. Do not touch uncovered PCB or connector metal without first discharging yourself!

Do not connect a receiver to the LVDS connector of the controller in slot 2 of the IPSO 19" Unit. The data will never be valid in this location.

A LVDS cable should never be removed from or connected to a powered controller. Corrupted data could be sampled as valid.

Do not connect more than one gradient amplifier to the same system.

**Mounting the DPP1 PCI Board**

2.3

The DPP1 board is intended to be mounted in a PCI environment. The driver is LINUX specific and will only work in an AVANCE III IPSO system.

DSP firmware is loaded from the TopSpin PC via the PCI bus and Ethernet.

All gradient values are transferred over two 48-bit LVDS interfaces.

The Next-Value (NV) clock signal is attached using a coax cable on the IPSO 19 inch case, or using a PCI connector pin on the IPSO AQS.

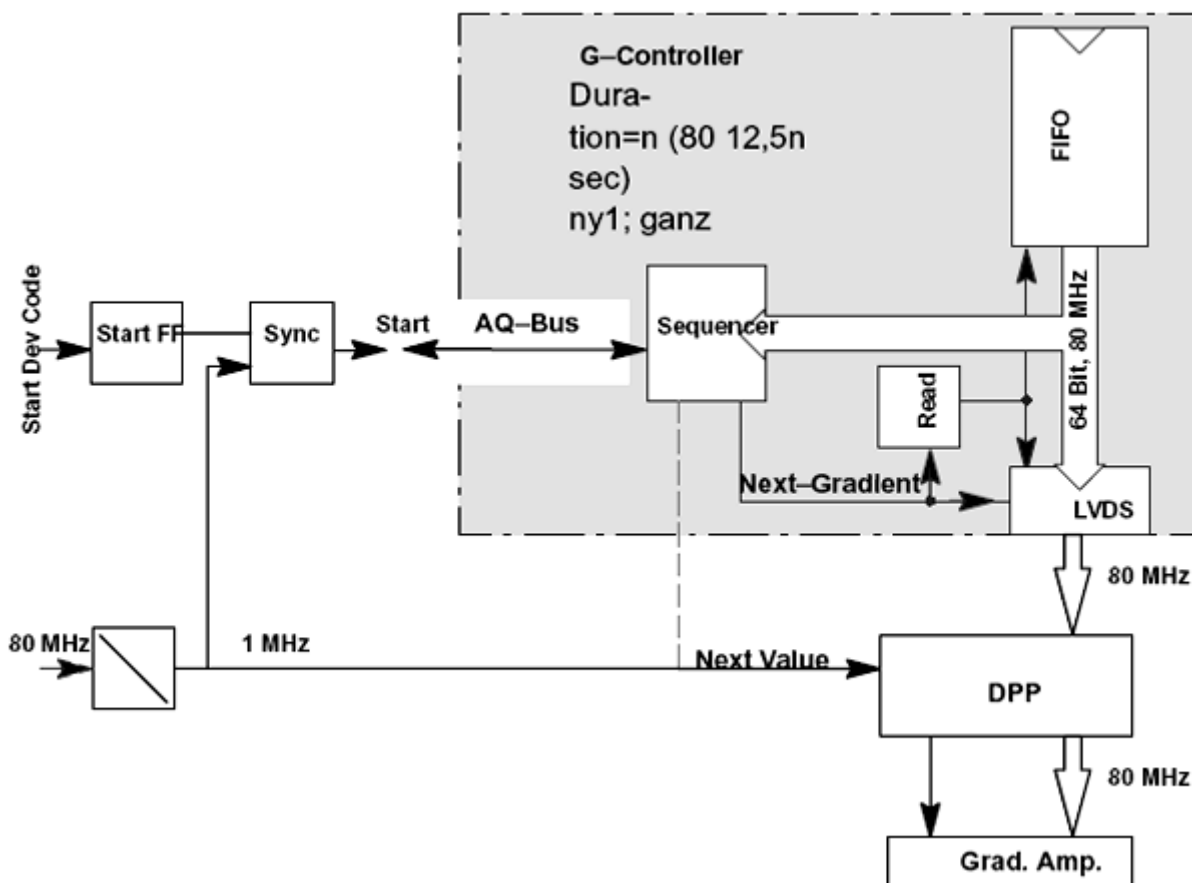


Figure 2.1. IPSO Functional Signal Flow

**Booting the DPP1**

2.4

The boot process starts after turning on the IPSO. The configuration is carried out beginning with post code "49" and LINUX begins to boot if the post code exceeds "60".

Recognition of the DPP1 during booting can be verified using the Web server on the IPSO or by using a browser on the TopSpin PC. The IPSO IP address, which is needed by the browser, can be located: in TopSpin, in the Hyper Terminal or in a shell on the workstation.

**In TopSpin:**

Type "ha" at the command line to display a dialog for all devices. Click on IPSO to open a browser with the IPSO's IP address.

**With Hyper Terminal:**

Type “**ifconfig**” at the IPSO prompt to display the IP address:

```
root@ipso:ifconfig
```

Enter this IP address in a standard browser’s URL field.

**In a Shell:**

Start a broadcast using “ping” and the parameters below will display the IP addresses of all the connected IPSO devices:

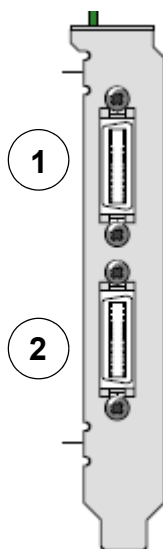
```
ping -w1 -b 149.236.99.255
```

Enter this IP address in the URL field of a standard browser.

**Proceeding in the browser:**

When you have entered the IP address in the browser the browser will display the “IPSO Service Web” page. Click consecutively on the following to show a list of all the controllers found as PCI devices. One of them will be the DPP1:

! Information      ! View Hardware List

**Ports****2.5**

1. 48-Bit LVDS Connector (26 pin) - OUTPUT to the Gradient Amplifier
2. 48-Bit LVDS Connector (26 pin) - INPUT from the Gradient Controller

Figure 2.2. Ports on the Front Panel of the DPP1

#### Data Output to Gradient Amplifier

- Low voltage, low noise LVDS output via 8 balanced data lines and one clock line.
- A transfer rate of 80 mega-words per second.
- A word width of 48 bits.

#### Data Input from Gradient Controller

- Low voltage, low noise LVDS input via 8 balanced data lines and one clock line.
- A transfer rate of 80 mega-words per second.
- A word width of 48 bits.

#### “Next Value” Clock from IPSO

When installed in the “IPSO 19” the DPP1 takes the “Next Value” clock via its ST1 connector connected to ST32 of the IPSO (IMB) using the cable H5516. In the “IPSO AQS” the DPP gets this clock signal via pin B14 of the PCI connector.

	IPSO 19“	IPSO AQS and Others
Source of the „Next Value“ Clock	ST1/H5516/St32	PCI B14

### Currents and Voltages

### 2.5.2

Part Number	+5 V	+ 3.3 V	+12 V	+5 VSB	-12 V
H12513F1	0	0.5 A	0	0	0

# Reference Numbers

# 3

Table 3.1. *Parts and Assemblies for the DPP1, H12513F1*

<b>Part Number</b>	<b>Drawing Number</b>	<b>Description</b>	<b>Version</b>
H12551F2	H4P2820b	PCB Layout	DPP1, ECL 01
H12551F3	H4P2820c	PCB Layout	DPP1, ECL 02/03/04
H12536		DPP1 Programming File	
HZ13694		DPP Slot Bracket	

Table 3.2. *Accessories*

<b>Part Number</b>	<b>Drawing Number</b>	<b>Description</b>
86868		48 Bit LVDS Cable, 1 meter
H5516		Coax Cable, 50 Ohm, SMB/SMB, 135 mm

## Reference Numbers

# Product Status and Modifications

# 4

## Introductory Status

4.1

Part Number	Name	Layout Number	Modification	Program File	Firmware	Jumper Setting
H12513F1	DPP1	H4P2820b	Yes		No	No

### Program File

The name of the program file includes the layout number and the EC level.

## Configuration and Settings

4.2

### Jumper Setting

There are no jumpers on this board. Some configuration settings have been made using zero Ohm resistors and should not be changed.

### PCI Bus

The following four resistors define the interrupt wiring.

Table 4.1. PCI Interrupt Selection

Signal	Mounted	Resistor	Comment
INT_A	Yes	R99	Interrupt to PCI on pin „A“
INT_B	No	R100	Not connected.
INT_C	No	RB30	Not connected.
INT_D	No	RB29	Not connected.

**LVDS Configuration**

Table 4.2. LVDS Identification Lines H12513F1 48 Bit Interface

Signal	LVDS Input	LVDS Output	Resistor Location	Comment
CHANNEL_DETECT_1	20	Not used	RB48	CHANNEL_DETECT = 00 G_CNTRL recognize connection to DPP
CHANNEL_DETECT_0	7	Not used	RB52	
USB pwr	19	19		These signals are connected between the input and output LVDS connector.
USB gnd	8	8		
USB +	1	1		
USB -	14	14		

**Firmware**

The firmware is loaded via PCI and Ethernet from the TopSpin PC as part of TopSpin. The DPP1 driver is a part of the “diskless” LINUX.

**Modification History**

**4.3**

Table 4.3. DPP1, H12513F1 Modification History

EC Number	Date	Layout Number	Description	Serial Number	EC Level
3461	21.9.06	H4P2820B	Introduction of the DPP1 for IPSO with 48 bit LVDS and external generation of NV clock.	0032 not shipped	00
3462	21.9.06		Removed the selection of NV clock input by a placement of a resistor. Due to a new termination, both inputs (coax connector for 19” and PCI pin for AQS) are ready to operate.	< 0041 not shipped	01
3463	21.9.06	H4P2820C	Removed the modifications from layout H4P2820B.	0100	02
3623	28.04.08		Corrected echo position jittering during imaging echo experiments.	0251	03

# Description

# 5

## Versions

5.1

Name	Part Number	EC Number	Firmware Number	Increments
DPP	H12513		No	28 Bit LVDS (test version)
DPP1	H12513F1	01	No	48 Bit LVDS
DPP1	H12513F1	02	No	Removing NV configuration

## Structure

5.2

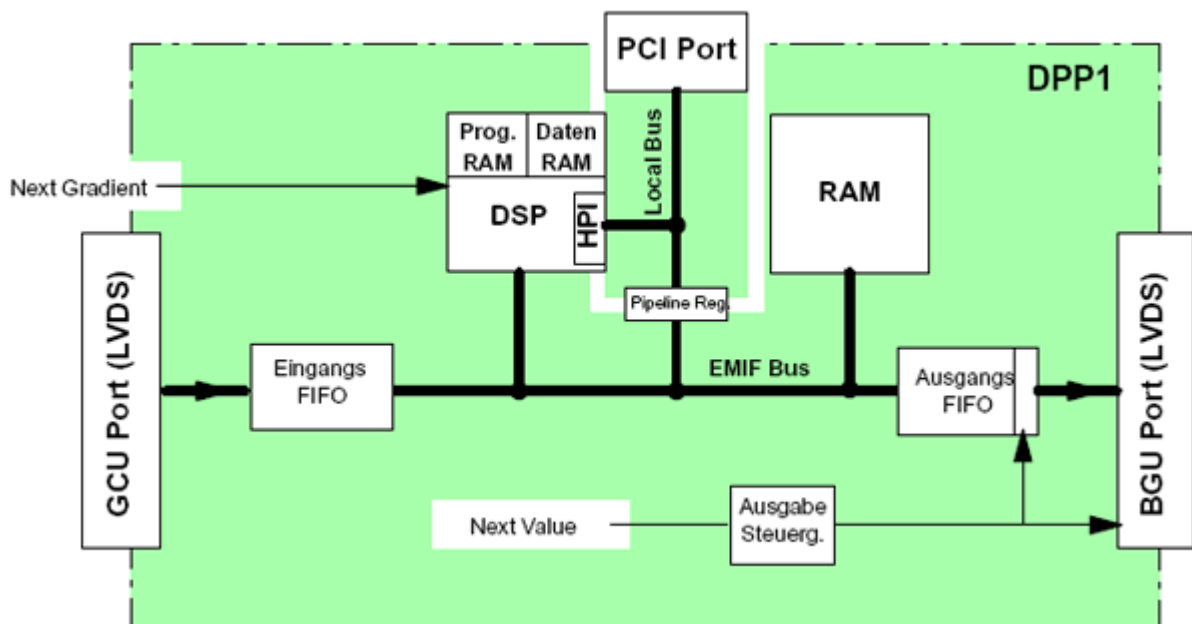


Figure 5.1: DPP1 Block Diagram

The PCI interface for the DPP1 is implemented using the PCI controller PCI9030 from PLX Technologies. The controller translates external PCI access to internal local bus access and vice versa. The local bus of the controller is connected to the mailbox register and the host port of the DSP.

### **Bus Structure**

The DPP1 has two independent bus systems:

- The **local bus**
- The DSP **External Memory Interface (EMIF) bus**

Each of these buses has its own address range. Exchanging data between the two busses is only possible via the DSP host port.

The DSP memory bus is attached to an external memory, as well as the LVDS input and output FIFO. The additional status register attached offers the possibility for the DSP to exchange data directly with the PCI bus.

The DPP1 control logic registers are also connected to the DSP memory bus.

### **Local Bus**

The local bus connects the DSP host port and the mailbox register to the PCI controller. The PCI controller performs the address mapping between the PCI and the local bus and provides the PCI bus port and the local bus port.

The PCI controller local bus has a bus width of 32 bit. The four memory regions are distributed into the following parts:

- Space 0 is reserved for the *Host Port Interface* of the DSP.
- Space 1 is reserved for logic registers.
- Space 2 resets the DSP.
- Space 3 is reserved for the FLASH memory.

### **EMIF Bus**

The DSP controls access from its host interface via the EMIF bus. The DSP memory (EMIF) bus is attached to an external memory, the DPP1 control logic, and the LVDS input and output FIFO's. The additional mailbox register attached offers the possibility of the DSP exchanging data directly with the PCI bus.

- Space 0 is reserved for the external memory of the DSP.
- Space 1 is reserved for the control logic and the pipeline register.
- Space 2 is reserved for the LVDS input FIFO
- Space 3 is reserved for the LVDS output FIFO.

### **DSP**

The DSP TMS320C6713B is a high performance floating point processor. When operating at 300 MHz the C6713B delivers up to 1800 MFLOPS.

**LVDS**

The data from the GCNTR to the DPP1 and from the DPP1 to the gradient amplifier is transmitted via two serial LVDS links. The word width transmitted is 48 bit and the word transfer speed is 80 MHz.

**FIFO's**

Each LVDS connection is connected to an input and output FIFO. The organization of the synchronous FIFO is 8192 x 36 bit.

**Memory**

The external synchronous SRAM on the EMIF bus of the DSP is 128 KB x 36 bit.

**Operation**

The Digital Preemphasis Processor (DPP) transmits new gradient data in a predefined time pattern to the gradient amplifier. In each time slot the software tests if a new data package is transferred from the GCU. The DSP reads the new data and uses it for the next calculation. If no new data set is available the output data to the gradient amplifier is calculated with a function of the old output data.

**Features**

- Floating point DSP *TMS320C6713* with internal:
  - Level 1 program cache (L1P) 4 KB.
  - Level 1 data cache (L1D) 4 KB.
  - Level 2 memory cache consists of 256 KB memory space that is shared between data and memory space.
- 128 KB x 36 bit expansion SRAM.
- PCI SMART Target I/O controller *PC19030*, 5 V I/O tolerant.
- 48 bit LVDS interface 80 MHz.
- Input/Output FIFO 8 KB x 36 bit.
- "Next Value" clock cycle is software programmable from 100 ns up to 1,023 sec.

**LVDS Data Structure****5.3**

The structure of the 48 bit word is identical at the receiver and transmitter.

## Description

Table 5.1: Word on the LVDS 48 bit 80 MHz Parallel Interface

Bit	48	47	...	44	43	...	38	37	...	22	21	...	18	17	...	6	5	4	3	2	1	
Field	P A R	MSB Address						MSB Data						Data (res)	(res)	!L A S T	! V A L I D	! N G				
		ADD<9..6>			ADD<5..0>			ADD<19..0>						gnd					gnd			
Number	1	4			6			16						4		12		1	1	1	1	1
Con- nected to DSP Data Bus or Logic	DSP Data Bus Bit:												not connected				DSP Bit	Logic				
	31	29..20						19..0											30			

Table 5.2: Bit Fields of the DPP Input and Output Word

Field	Value	Description
!NG		Next gradient bit; high active in FIFO; low active on the LVDS interface.
	0	Leads only to the Next gradient, the word does not contain data, !Valid=0 in the same 48 bit word was an error.
	1	!Valid=0 and Out=1 means a gradient value is transferred without the Next gradient.
!VALID		Gradient data valid bit; high active in FIFO; low active on the LVDS interface.
	0	The word contains only data and no „Next Gradient“. !NG=0 in the same word was an error.
	1	There is no gradient data in this word.
PAR		Parity bit, even parity, bit sum over the bits 1 to 47 (DPP only). The DPP1 is software controlled.
!LAST	0	The last word in the gradient package is marked with !NG=0 or !VALID=0; high active in FIFO; low active on the LVDS interface.

The LVDS interface always sends a default word (Last word; NG=1; !Valid=1) even if no gradient or NEXT gradient words transfers. With the default word, the load bits, Valid and NG bit are inactively set to =1.

Bit	48	47	46	45	44	43	42	...	33	32	...	17	18	...	1
Field	PAR	Default word of the idle state.													
Value	1	Last word = 1													

## Software Interface

5.4

### PCI Bus Interface

5.4.1

#### PCI Configuration Space

The values of these registers are loaded out of the EEPROM at power-up, together with some values from the local bus configuration registers.

Configuration Space Address	Register Description	Bits	Register Values	Value Description
02h	Device ID	[31:16]	9030 h	
00h	Vendor ID	[15:0]	10B5 h	
06h	PCI Status	[31:16]	0010 h	
04h	PCI Command	[15:0]	0000 h	
0Ah	Class Code	[31:8]	0680 00 h	
08h	Revision	[7:0]	000A h	
10 h	Base Address 0: Memory access to Local Bus Configuration Register	[31:0]	FFFF FF80 h	128 byte
14 h	Base Address 1: I/O access to Local Bus Configuration Register	[31:0]	FFFF FF80 h	128 byte
18 h	Base Address 2: Memory access to Local Bus CS0	[31:0]	FFF0 0000 h	1MB range
1C h	Base Address 3: Memory access to Local Bus CS1	[31:0]	FFFF 0000 h	64K range
20 h	Base Address 4: Memory access to Local Bus CS2	[31:0]	FFFF 0000 h	64K range
24 h	Base Address 5: Memory access to Local Bus CS3	[31:0]	FFFF 0000 h	64K range
28 h	Not supported			

## Description

2Eh	Subsystem ID	[31:16]	0000 h	
2Ch	Subsystem Vendor ID	[15:0]	0000 h	
36h	MSB New Capability Pointer		0000 h	Reserved
34h	LSB New Capability Pointer	CAP_PTR[7:0]	0040 h	
3Eh	Maximum Latency & min. Grant		0000 h	Not loadable
3Ch	Interrupt Pin/Line	[15:0]	01FF h	
42h	MSW of Power Management Capabilities	PMC [15:11,5,3:0]	4801 h	
40h	LSW of Power Management Next Capability pointer	PMNEXT [7:0] PMCCA- PID[7:0]	4801 h	
46h	MSW of Power Management data		0000 h	Reserved
44h	LSW of Power Management Control / Status	PMCSR [14:8]/ PCIILR [7:0]	0000 h	
4Ah	MSW of Hot Swap / Control		0000 h	Reserved
48h	LSW of Hot Swap Next Capability Pointer / Control	HS_NEXT[7:0] HS_CNTL[7:0]	4C06	
4Eh	PCI Vital Product Data Address		0000 h	Reserved
4Ch	PCI Vital Product Data Next Capability Pointer / Control	PVPD_NEXT[ 7: 0] PVPD- CNTL[7:0]	0003 h	

### PCI Software Interface

### 5.4.2

After power-up, the PCI address map of the internal DPP addresses at the local bus is created by the BIOS using the contents in the configuration registers "base address 0...5". The results are the PCI base addresses for the local bus chip selects which are written into the same configuration registers by BIOS.

Table 5.3: PCI Local Bus Addresses

External PCI Bus Access				Local Bus Access		
Access type	Range	Address	PCI Address	Local Address	Destination	
Memory: non-prefetch	1 MB	Bit [31...20]	<PCI Base2>	<LAS0BA>=0xxh	CS0; Addr=0xxh Range=256B	DSP Host Port, 2 Register
		Bit [19...0]	PCI AD [19...0]			
Memory: non-prefetch	64kB	Bit [31...16]	<PCI Base3>	<LAS1BA>=02xxh	CS1; Addr=2xxh Range=256B	1 Mailbox register
		Bit [15...0]	PCI AD [15...0]			
Memory: non-prefetch	64 kB	Bit [31...16]	<PCI Base4>	<LAS2BA>=04xxh	CS2; Addr=4xxh Range=256B	1 DSP Reset
		Bit [15...0]	PCI AD [15...0]			
Memory: non-prefetch	64 kB	Bit [31...16]	<PCI Base5>	<LAS3BA>=1xxxxh	CS3; Addr=1xxxxh Range=64kB	Flash Prom
		Bit [15...0]	PCI AD [15...0]			
Memory: non-prefetch	128 B	Bit [31...7]	<PCI Base0>	none	Internal Register Range=128B	32 Local Bus Config Register
		Bit [6...0]	PCI AD [6...0]			
I/O	128 B	Bit [31...7]	<PCI Base1>	none	Internal Register Range=128B	32 Local Bus Config Register

Values in the column “External PCI Bus Access” depend on the content of the “PCI Base Address Register” read by the BIOS after power-up.

Values in the column “Local Address” depend on the content of the “Local Base Address Remap Registers”.

Values in the column “Destination” depend on the content of the “Local Bus Chip Select Registers”.

## Description

### **Local Bus Interface**

The PCI controller provides 4 chip select signals on its local bus side to access different address spaces.

Table 5.4: Local Bus Chip Select Signals Usage

PCI9030 Chip Select Signals	Usage	Address Range
PLX CS 0	DSP HPI	
PLX CS 1	Pipeline Register	
PLX CS 2	DSP Reset	
PLX CS 3	Flash Memory	

Table 5.5: Local Bus Chip Select Registers

PCI Address Offset	Register Description	Register Name	Register Values	Register Value Description
3C h	Chip Select 0 Base Address	CS0BASE	0000 0081 h	CS0 enabled; Addr=0xxh Range=256B
40 h	Chip Select 1 Base Address	CS1BASE	0000 0281 h	CS1 enabled; Addr=2xxh Range=256B
44 h	Chip Select 2 Base Address	CS2BASE	0000 0481 h	CS2 enabled; Addr=4xxh Range=256B
48 h	Chip Select 3 Base Address	CS3BASE	0001 8001 h	CS3 enabled; Addr=1xxxxh Range=64kB

### **Local Bus Configuration Registers**

5.4.3

Table 5.6: Local Bus Configuration Registers

PCI Address Offset	Register Description	Register Name	Register Values	Register Value Description
00h	Local Address Space 0 Range	LAS0RR	FFF0 0000 h	1MB Byte Local Memory Space, non-prefetch
04h	Local Address Space 1 Range	LAS1RR	FFFF 0000 h	64kB Byte Local Memory Space, non-prefetch
08h	Local Address Space 2 Range	LAS1RR	FFFF 0000 h	64kB Byte Local Memory Space, non-prefetch

Table 5.6: Local Bus Configuration Registers

0C h	Local Address Space 3 Range	LAS1RR	FFFF 0000 h	64 kB Local Memory Space, non-prefetch
10 h	Expansion Rom Range	EROMRR	0000 h	Disable
14 h	Local Address Space 0 Local Base Address (Remap)	LAS0BA	0000 0001 h	enable CE 0; Base=0h
18 h	Local Address Space 1 Local Base Address (Remap)	LAS1BA	0000 0201 h	enable CE 1; Base=200h
1C h	Local Address Space 2 Local Base Address (Remap)	LAS2BA	0000 0401 h	enable CE 2; Base=400h
20 h	Local Address Space 2 Local Base Address (Remap)	LAS3BA	0001 0001 h	enable CE 3; Base=10000h
24 h	Expansion Rom Local Base Address (Remap)	EROMBA	0001 0000 h	Disable
28 h	Local Address Space 0 Bus Region Descriptor	LAS0BRD	4040 0022 h	Ready Input enable 16 Bit Local Bus Width
2C h	Local Address Space 1 Bus Region Descriptor	LAS1BRD	4040 8820 h	16 Bit Local Bus Width, NRDD 1, NWAD 1, Write Hold 1
30 h	Local Address Space 2 Bus Region Descriptor	LAS2BRD	4040 8820 h	16 Bit Local Bus Width, NRDD 1, NWAD 1, Write Hold

## Description

Table 5.7: Local Bus Control Registers

PCI Addr. Offset	Register Description	Register Name	Register Values
4C	Interrupt Control / Status	INTCSR	0030 0048 h
50 h	PCI Target Response, Serial EE-PROM, Initialization Control	CNTRL	1078 0000 h
54 h	General Purpose I/O Control	GPIOC	0024 EB40 h
70 h	Hidden 1 Power Management Data Select	PMDATA	0 h
74 h	Hidden 2 Power Management Data Scale	PMCSR[14:13] hidden, PMCSR[7:0] used	0 h

### Local Bus Address Map

5.4.4

Table 5.8: Local Bus Address Map

Acronyms	Local Address	Space	Function	Mode R/W	Bit
	0000	CS0	DSP HPI Control Register low word	R/W	15–0
	0002	CS0	DSP HPI Control Register high word	R/W	15–0
	0004	CS0	DSP HPI Address Register low word	R/W	15–0
	0006	CS0	DSP HPI Address Register high word	R/W	15–0
	0008	CS0	DSP HPI Data Register low word	R/W	15–0
	000A	CS0	DSP HPI Data Register high word	R/W	15–0
	0000	CS1	Pipeline Register	W	31–0
	0000	CS2	DSP Reset	W	xxxx
	0000 – FF	CS3	Flash Memory	W/R	15–0

### Flash Prom at the Local Bus

5.4.5

Bus characteristics for accessing Flash PROM's:

Bus width: Two byte, data bit 7...0 attached; data bit 15...8 not used; therefore the flash prom occupies the double address area.

Cycle Control: Clock controlled.

Cycle Length: Approximately 85 nanoseconds for posting and 270 nanoseconds for the reading cycle.

Table 5.9: Type of Flash Proms used on the DPP

Local Hex Address	Size (KByte)	Word (Byte)	Type	Type of Controller
C000 0000 - C000 00FF	64	1 Byte		DPP1 H12513F

**Registers at the Local Bus****5.4.6**

Table 5.10: DSP HPI Register

0000	CS0	DSP HPI Control Register low word.	R/W	15–0
0002	CS0	DSP HPI Control Register high word.	R/W	15–0
0004	CS0	DSP HPI Address Register low word.	R/W	15–0
0006	CS0	DSP HPI Address Register high word.	R/W	15–0
0008	CS0	DSP HPI Data Register low word.	R/W	15–0
000A	CS0	DSP HPI Data Register high word.	R/W	15–0
000C	CS0	DSP HPI Data Register low word with address auto increment.	R/W	15–0
000E	CS0	DSP HPI Data Register high word with address auto increment.	R/W	15–0

The host port interface needs a sequence to read or write to the DSP. The host begins HPI access by performing the following tasks in this order:

- Initializing the HPI control register (HPIC).
- Initializing the HPI address register (HPIA).
- Writing data to or reading data from the HPI data register (HPID).

Table 5.11: DSP HPI Control Register Host View

Bits	31	..	20	19	18	17	16	1	5	..	4	3	2	1	0
Field	Reserved			Reser ved	HINT	DSPI NT	HWO B	Reserved			Rese rved	HINT	DSPI NT	HW OB	
HOST read/ write	HR			HR	HR/W	HR/W	HR/W				HR	HR/ W	HR/ W	HR/ W	
Reset State	0			X	0	0	0	0			X	0	0	0	

## Description

Table 5.12: DSP HPI Control Register CPU View

<b>Bits</b>	31	..	20	19	18	17	16	15	..	4	3	2	1	0
<b>Field</b>	Reserved						Reserved				HRDY	HINT	DSPIN	HWOB
<b>CPU read/write</b>	R						R				R	R/W	R/W	R/W
<b>Reset State</b>	0						0				1	0	0	0

For a detailed description see Texas Instruments Host Port Interface Reference Guide (SPRU578C).

### Pipeline Register

The pipeline register is used by the software to monitor and control the DPP activities. It is available for the DPP and the host computer and used so that the register can read and write at the same time. When the DSP writes to the register an interrupt on the host computer is activated that requests this data to be read. The same occurs in reverse.

Table 5.13: DPP Pipeline Register

<b>Bits</b>	31	..	10	9	8.. 5	4	3	2	1	0
<b>Field</b>		not used		ERROR	not used	INTR	OUTPUT	INPUT	IDLE	ACTIVE
<b>Reset State</b>	0	0	0	0	0	0	0	1	0	0

Table 5.14: Field Description of the Mailbox Register

Field	Value	Description
0	1	ACTIVE, DPP is up and Firmware is running.
1	1	IDLE, DPP is up but nothing to do.
2	1	INPUT, DPP read from input buffer.
3	1	OUTPUT, DPP write to output buffer.
4	1	INTR, DPP has send Interrupt.
9	1	ERROR, DPP detected error, info in mailbox.

**DSP Reset**

0000 0000	CS2	DSP Reset	W	xxxx
-----------	-----	-----------	---	------

The DSP is reset by writing any data on address zero in the local region 2 of the PCI smart target accelerator. The reset has no effect on the control logic.

**Local Address Layout**

5.4.7

**Local Bus Chip Select Usage**

Table 5.15: Local Bus Memory Regions

PLX Select Signal	DSP Memory Allocation	Module
PLX CS 0		DSP HPI
PLX CS 1	DSP CE1	Pipeline Register
PLX CS 2		DSP Reset
PLX CS 3		Flash Memory

**The DSP 6713**

5.4.8

**DSP Boot Mode and Configuration**

The C6713 uses a variety of boot configurations to determine what actions the device is to perform after reset for proper device initialization.

The table below describes the device configuration pins, which are set up via internal or external pull-up/pull-down resistors through the HPI data pins, and CLKMODE0 pin. These pins must be in a desired state until reset is released.

Table 5.16: DSP Configuration Pins

Configuration Pin	Connect to	Description
HD 12	1	<p>EMIF Big Endian mode correctness [C6713B]</p> <p>0 – The EMIF data will always be presented on the ED (7:0) side of the bus, regardless of the Endianess mode (Little / Big Endian).</p> <p>1 – In Little Endian mode (HD8 = 1), the 8 bit or 16 bit EMIF data will be present on the ED (7:0) side of the bus.</p> <p>In Big Endian mode (HD8 = 0), the 8 bit or 16 bit EMIF data will be present on the ED (31:24) side of the bus [default].</p>

## Description

Table 5.16: DSP Configuration Pins

HD8	1	Device Endian mode 0 – The system operates in Big Endian mode. 1 – System operates in Little Endian mode [default].
HD[4:3]	00	Boot mode configuration pins 00 – CE1 width 32-bit, HPI boot/ Emulation boot 01 – CE1 width 8-bit, asynchronous external ROM boot with default timings [default mode] 01 – CE1 width 16-bit, asynchronous external ROM boot with default timings [default mode] 01 – CE1 width 32-bit, asynchronous external ROM boot with default timings [default mode].
CLKMODE0	1	Clock generator input clock source select 0 – Reserved 1 – CLKIN square wave [default].

### DSP Defined Address Ranges

Table 5.17: DSP Address Map

Memory Block Description	Block size (Bytes)	Hex Address Range
Internal Ram (L2)	192 K	0000 0000 – 0002 FFFF
Internal Ram / Cache	64 K	0003 0000 – 0003 FFFF
Reserved	24M – 256K	0004 0000 – 017F FFFF
EMIF Register	256 K	0180 0000 – 0183 FFFF
L2 Registers	128 K	0184 0000 – 0185 FFFF
Reserved	128 K	0186 0000 – 0187 FFFF
HPI Registers	256 K	0188 0000 – 018B FFFF
McBSP 0 Registers	256 K	018C 0000 – 018F FFFF
McBSP 1 Registers	256 K	0190 0000 – 0193 FFFF
Timer 0 Registers	256 K	0194 0000 – 0197 FFFF
Timer 1 Registers	256 K	0198 0000 – 019B FFFF
Interrupt Selector Registers	512	019C 0000 – 019C 01FF

Table 5.17: DSP Address Map

Device Configuration Registers	4	019C 0200 – 019C 0203
Reserved	256 K – 516	019C 0204 – 019F FFFF
EDMA Ram & EDMA Registers	256 K	01A0 0000 – 01A3 FFFF
Reserved	768 K	01A4 0000 – 01AF FFFF
GPIO Registers	16 K	01B0 0000 – 01B0 3FFF
Reserved	240 K	01B0 4000 – 01B3 FFFF
I2C0 Registers	16 K	01B4 0000 – 01B4 3FFF
I2C1 Registers	16 K	01B4 4000 – 01B4 7FFF
Reserved	16 K	01B4 8000 – 01B4 BFFF
McASP0 Registers	16 K	01B4 C000 – 01B4 FFFF
McASP1 Registers	16 K	01B5 0000 – 01B5 3FFF
Reserved	160 K	01B5 4000 – 01B7 BFFF
PLL Registers	8 K	01B7 C000 – 01B7 DFFF
Reserved	264 K	01B7 E000 – 01BB FFFF
Emulation Register	256 K	01BC 0000 – 01BF FFFF
Reserved	4 M	01C0 0000 – 01FF FFFF
QDMA Registers	52	0200 0000 – 0200 0033
Reserved	16 M – 52	0200 0034 – 02FF FFFF
Reserved	720 M	0300 0000 – 2FFF FFFF
McBSP 0 Data Port	64 M	3000 0000 – 33FF FFFF
McBSP 1 Data Port	64 M	3400 0000 – 37FF FFFF
Reserved	64 M	3800 0000 – 3BFF FFFF
McASP 0 Data Port	1 M	3C00 0000 – 3C0F FFFF
McASP 1 Data Port	1 M	3C10 0000 – 3C1F FFFF
Reserved	1 G + 62 M	3C20 0000 – 7FFF FFFF
EMIF CE0	256 M	8000 0000 – 8FFF FFFF
EMIF CE1	256 M	9000 0000 – 9FFF FFFF
EMIF CE2	256 M	A000 0000 – AFFF FFFF
EMIF CE3	256 M	B000 0000 – BFFF FFFF
Reserved	1 G	C000 0000 – FFFF FFFF

**The DSP External Memory Interface (EMIF)**

The DSP EMIF support a glue-less interface to a variety of external devices, including:

- Pipe lined synchronous burst SRAM (SBSRAM).
- Synchronous DRAM (SDRAM).
- Asynchronous devices, including SRAM, ROM and FIFO's.

If multiple requests arrive simultaneously, the EMIF prioritizes them and performs the necessary number of operations. The behavior of the EMIF is defined in dedicated registers.

*Table 5.18: EMIF Control Register*

<b>Register Name</b>	<b>Address</b>	<b>Value</b>	<b>Comment</b>
Global Control reg.	0 x 180 0000	0 x 0000 30F8	
Space control reg. CE 0	0 x 180 0008	0 x FFFF FF43	32 bit SBRAM
Space control reg. CE 1	0 x 180 0004	0 x 1221 C222 0 x 1091 4221 possible	32 bit asyn. RAM
Space control reg. CE 2	0 x 180 0010	0 x FFFF FF43	32 bit SBRAM
Space control reg. CE 3	0 x 180 0014	0 x FFFF FF43	32 bit SBRAM

*Table 5.19: Bit Description of EMIF Space CE Control Register*

<b>Bit 31..28</b>	<b>Bit 27..22</b>	<b>Bit 21..20</b>	<b>Bit 19..16</b>
Write setup	Write strobe	Write hold	Read setup
RW, +1111	RW, +111111	RW,+ 11	RW, + 1111

<b>Bit15..14</b>	<b>Bit 13..8</b>	<b>Bit 7..4</b>	<b>Bit 3</b>	<b>Bit 2..0</b>
TA	Read strobe	MTYPE	Write hold MSB(1)	Read hold
RW, +1111	RW, +111111	RW,+ 11	RW, + 0	RW, + 011

Table 5.20: EMIF Space Control Register Field Description

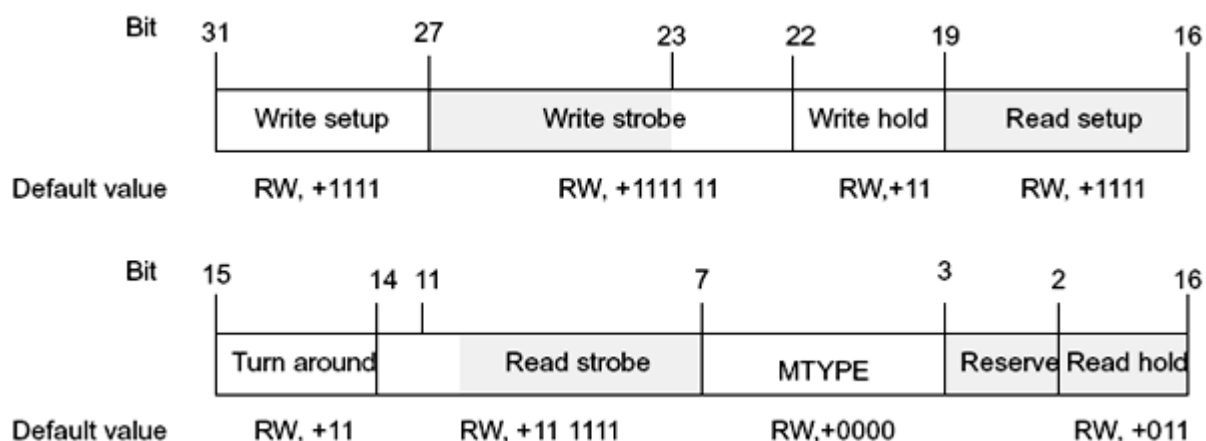


Table 5.21: EMIF CE Space Control Register Field Description

Field	Description
Read setup Write setup	Setup width. Number of clock cycles of setup time for address (EA), chip enable (CE), and byte enables (BE 3..0) before strobe or write strobe falls. For asynchronous read accesses, this is also the setup time of AOE before ARE falls.
Read strobe Write strobe	Strobe width. The width of the read strobe (ARE) and write strobe in clock cycles.
Read hold Write hold	Hold width. Number of clock cycles that address (EA) and byte strobes (BE (3..0)) are held after read strobe or write strobe rises. For asynchronous read accesses, this is also the hold time of AOE after ARE rising.
MTYPE	Definition for C671x.
	MTYPE = 0100: 32-bit wide SBSRAM.
	MTYPE = 1010: 8-bit wide SBSRAM.
	MTYPE = 1011: 16-bit wide SBSRAM.
TA	The turn around time controls the number of ECLKOUT cycles between a read and write, or between reads, to different CE spaces (asynchronous memory types only).

The MTYPE field identifies the memory type for the corresponding CE space. If the MTYPE field selects a synchronous memory type (SBSRAM), the remaining fields of the register have no effect.

### The DSP PLL Register

The DSP includes a PLL and a flexible PLL controller peripheral consisting of a pre-scale (D0) and four dividers (OSCDIV1, D1, D2, D3). The PLL controller is able to generate different clocks for different parts of the system (DSP core, external memory interface and other peripherals). The picture below illustrates the PLL and clock generation logic.

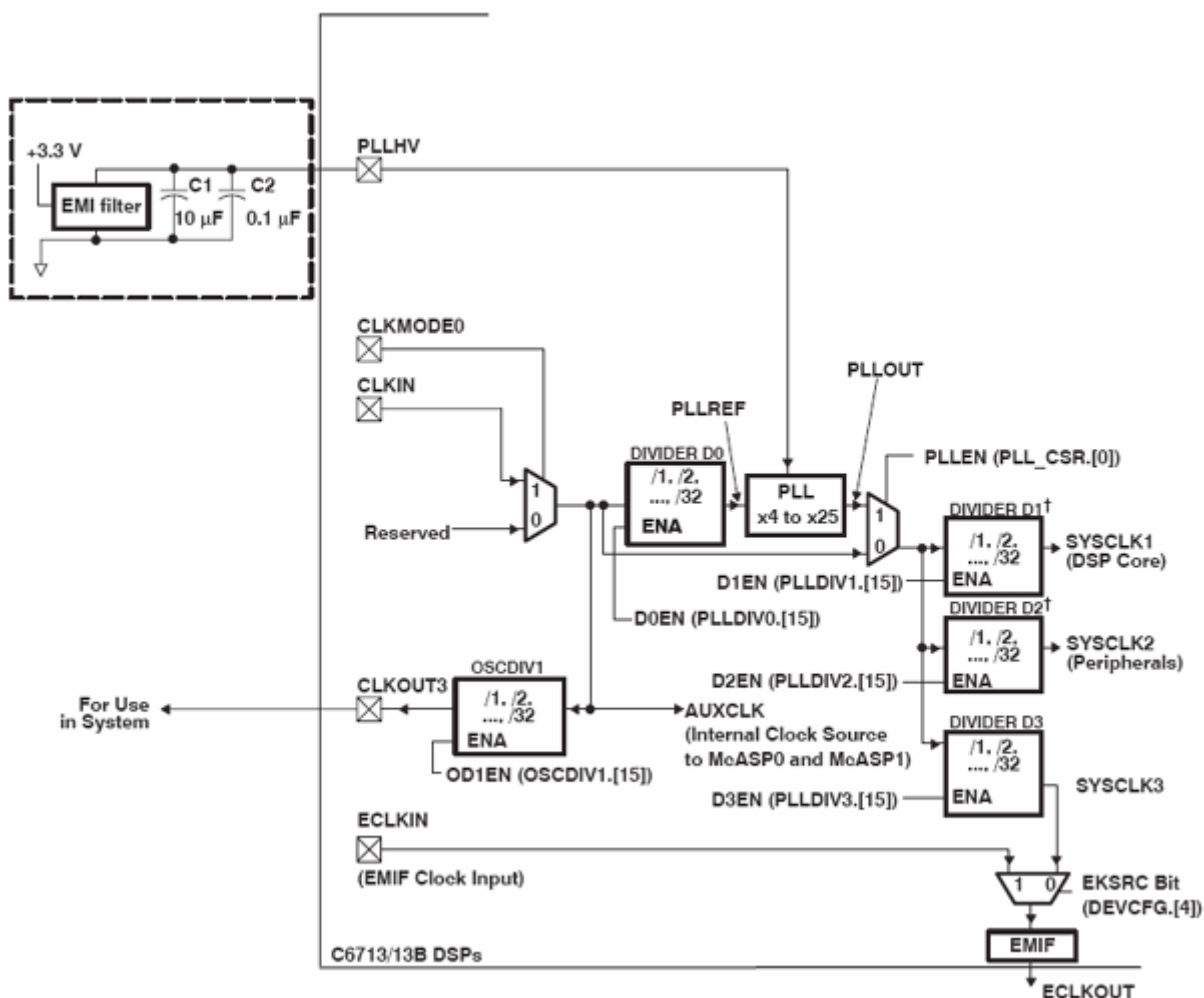


Figure 5.2: PLL Register Structure

All registers must be initialized by software after reset. The PLL controller registers should be modified only by the CPU, and as soon as possible at the beginning of the program.

Table 5.22: PLL Register Contents

Register Name	Address	Value	Comment
PLLM	0x1B7C110	0xb	CLKIN x 11
PLLDIV 0	0x1B7C114	0x8000	Divide by 1
PLLDIV 1	0x1B7C118	0x8000	Divide by 1
PLLDIV 2	0x1B7C11C	0x8001	Divide by 2
PLLDIV 3	0x1B7C120	0x8002	Divide by 3
PLLCSR	0x1B7C100	0x40	Quit reset
PLLCSR	0x1B7C100	0x41	Enable PLL

**Configuration of Interrupts****5.4.9**

Interrupts to the DSP can be released by the internal events of the DPP logic Next value, delayed gradient flag (GFD) and calculation time-out, or by setting the corresponding bit in the mailbox register via the PCI bus and PCI controller (PLX).

Table 5.23: DSP Enable Register

DSP Register Name	Address	Value	Function
GPEN	01B0 0000	0xF0	No GPIO pin
GPPOL	01B0 0024	0x40	Polarity

Refer to the SPRU 190D technical manual, chapter 17.4.1, for more information.

Table 5.24: Allocation of DSP Interrupts

DSP Interrupt Input	Source Signal	Function	Active Level
INT 4	INT	INT	High
INT 5	GFD	GFD	High
INT 6	IWR_DSP	Logic to DSP: „Read Pipeline Register“	High
INT 7	CNT_ERR	Calculation error counter > time-out value	High

#### **Interrupts from Logic or DSP to Host**

Interrupts to the host can be released by the DSP host port interrupt (HINT to LINT1 of the PCI controller) or by setting the corresponding bit in the Mailbox Register (to LINT2 of the PCI controller) via the EMIF Bus. Both interrupts can only be initiated by the DSP.

The PCI controller interrupt inputs LINT1 and LINT2 are routed to the PCI connector pin INT A.

The PLX controller interrupt inputs are routed to the PCI bus INT A.

## Description

Table 5.25: PLX Controller Interrupts

DSP Interrupt Input	Source Signal	Function	Active Level
LINT 1	HINT	DSP to Host interrupt	Low
LINT 2	IWR_PLX	Logic to Host: „Read Pipeline Register“	High

### Configuration of the External Memory Interface (EMIF)

The DSP EMIF supports a glue-less interface to a variety of external devices, including:

- Pipe-lined synchronous–burst SRAM (SBSRAM).
- Synchronous DRAM (SDRAM).
- Asynchronous devices, including SRAM, ROM and FIFO's.

If multiple requests arrive simultaneously, the EMIF prioritizes them and performs the necessary number of operations. The behavior of the EMIF is defined in some dedicated registers.

### Content of EMIF Register and Resulting Memory Allocation

Table 5.26: Configuration Register and Resulting Memory Allocation

Register Name	Configuration Register		Memory Type	Memory allocation		
	Hex Address	Hex Value		DSP Select Signal	DSP Address	Device
Global Control Register	180 0000	0000 30F8				
Space control reg. CE 0	180 0008	FFFF FF43	32 bit SBRAM	DSP CE 0	80000000 – 8000FFFF	Memory
Space control reg. CE 1	180 0004	1081 0220	32 bit asyn. RAM	DSP CE 1	90000000 – 90000008	Control Register
Space control reg. CE 2	180 0010	FFFF FF43	32 bit SBRAM	DSP CE 2	A0000000	Receiver FIFO
Space control reg. CE 3	180 0014	FFFF FF43	32 bit SBRAM	DSP CE 3	B000 0000	Output FIFO

**Description of the Global Control Register**

GBLCTL	0180 000	Global Control Register	R/W	31-0
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The EMIF global control register configures the common parameters to all memory spaces.

Table 5.27: Bit Fields of the Space Control Register

<b>Bits</b>	31..14	13	12	11	10	9	8
<b>Fields</b>	reserved			BUS-REQ	ARDY	HOLD	HOLDA
<b>Res.</b>	0	1	1	0	0	0	0
<b>Bits</b>	7	6		5	4	3	2..0
<b>Fields</b>	NOHOLD	reserved		EKEN	reserved	CLK2EN	reserved
<b>Res.</b>	0	1		1	1	1	0

Table 5.28: Bit Field Description

Field	Value	Description
31..12	Reserved	A value written to these bit field locations has no effect.
11	BUSREQ	The bus request output bit indicates if the EMIF has an access / refresh pending or in progress. 0 BUSREQ output is low. No access / refresh pending. 1 BUSREQ output is high. Access / refresh pending or in progress.
10	ARDY	Input bit. 0 External devices is not ready. 1 External devices is ready.
9	HOLD	Input bit. 0 External device requesting EMIF. 1 No external request pending.
8	HOLDA	Input bit. 0 External device owns EMIF. 1 External device does not own EMIF.
7	NOHOLD	Enable bit. 0 No hold is disabled. Hold request via the HOLD input are acknowledge via the HOLDA output at the earliest possible time. 1 No hold is enabled. Hold request via the HOLD input are ignored.

## Description

Table 5.28: Bit Field Description

6	Reserved	A value written to this bit field location has no effect. The reserved bit location is always read as 1.
5	EKEN	Enable bit. 0 ECLKOUT is held low. 1 ECLKOUT is enabled to clock (default).
4	CLK1EN	Enable bit 0 Not available on C6713. This bit must be programmed to zero for proper operation.
3	CLK2EN	Enable / disabled using SSCEN / SDCEN bits. 0 CLKOUT2 is held high. 1 CLKOUT2 is enabled to clock (default).
31..12	Reserved	A value written to this bit field location has no effect. The bit field is always read as 0.

### Description of the Global Control Register

CECTL0	0180 000	Global Control Register for CE0	R/W	31-0
CECTL1	0180 000	Global Control Register for CE1	R/W	31-0
CECTL2	0180 000	Global Control Register for CE2	R/W	31-0
CECTL3	0180 000	Global Control Register for CE3	R/W	31-0

The space control registers correspond to the CE memory spaces supported by the EMIF. There are four CE space control registers that correspond to the four external CE signals. The MTYPE field identifies the memory type for the corresponding CE space. If the MTYPE field selects an asynchronous type, the remaining register fields specify the shaping of the address and control signals for the access to that space. The MTYPE field should only be set during system initialization. The exception is when CE1 is used for the ROM boot mode. In this case the CE space can be configured to another asynchronous memory type.

Table 5.29: Bit Fields for the Space Control Register

<b>Bits</b>	3 1	..	2 8	2 7	..	2 2	2 1	2 0	1 9	..	1 6	1 5	1 4	1 3	..	8	7	..	4	3	2	1	0
<b>Fields</b>	Write setup		Write strobe		Write hold		Read setup		TA		Read strobe		MTYPE		r	e	s	Read hold					
<b>Res.</b>	1111		111111		11		1111		11		111111		0000		0	011							

Table 5.30: Bit Field Description

Field	Value	Description
Write setup	1111	Number of clock cycles of setup time for address (EA), chip enable (CE), and byte enables (BE 3..0) before the write strobe falls. For asynchronous read access, this is also the setup time of AOE before ARE falls.
Read setup	111111	Number of clock cycles of setup time for address (EA), chip enable (CE), and byte enables (BE 3..0) before the read strobe falls. For asynchronous read access, this is also the setup time of AOE before ARE falls.
Write strobe	111111	The write strobe width in number of clock cycles.
Read strobe	111111	The read strobe width in number of clock cycles.
Write hold	11	The number of clock cycles that address (EA) and byte strobes (BE 3..0) are held after the write strobe rises. For asynchronous read access, this is also the hold time of AOE after ARE rising.
Read hold	11	The number of clock cycles that address (EA) and byte strobes (BE 3..0) are held after the read strobe rises. For asynchronous read access, this is also the hold time of AOE after ARE rising.
MTYPE	1010 1011 0100	Memory type definition: 8-bit wide SBSRAM 16-bit wide SBSRAM 32-bit wide SBSRAM
TA	11	Turn around time: Controls the number of ECLKOUT cycles between a read and write, or between reads, to different CE spaces (asynchronous memory types only).

The MTYPE field identifies the memory type for the corresponding CE space. If the MTYPE field selects a synchronous memory type (SBSRAM), the remaining fields of the register have no effect.

### External Memory at EMIF, Space CE0

### 5.4.9.3

The DSP is connected to an external synchronous SRAM. This memory chip is organized as 128K x 36 bit.

Table 5.31: Type of External Memory

Local Hex Address	Size [KByte]	Word [Byte]	Type	Bandwidth [MByte/s]	Type of Controller	Identification
8000 0000 – 8007 FFFF	512	4 Byte	SRAM	400	DPP H12513F1	subdev=???

The LVDS input and output FIFO is a high density synchronous 36 bit FIFO. Only the lower 32 bits are connected to the EMIF bus of the DSP. If the LVDS words have a legal valid bit, the information is written into the input FIFO.

Table 5.32: Bit Allocation at the EMIF Bus

<b>Bit</b>	4 8	47..44	43..38	37..22	21..18	17..6	5	4	3	2	1
<b>Field</b>	P A R	MS B Address		MS B Data		Data (res)	(res)		!LAST	!V A L I D	!N G
		ADD<9..6>	ADD<5..0>	DATA <19..0>		gnd	gnd				
<b>Number</b>	1	4	6	16	4	12	1	1	1	1	1
<b>Conne cted to DSP Data Bus or Logic</b>	DSP Data Bus Bit					Not connected			DSP Bit	Logic	
	3 1	29..20		19..0					30		

The input FIFO and output have a size of 36 bits x 8192 words.

Table 5.33: Type of FIFO's Used on the DPP1

Local Hex Address	Size [KByte]	Word [Byte]	Type	Bandwidth [MByte/s]	Type of Controller	Identification
Axxx xxxx	128	4 Byte		200	DPP1 H12513F1	Receiver FIFO
Bxxx xxxx	128	4 Byte		200	DPP1 H12513F1	Transmit FIFO

**DSP Address Map****5.4.10***Table 5.34: Memory Region of EMIF Bus*

DSP Select Signal	DSP Memory Allocation	Module
DSP CE 0	0x80000000 - 0x8000FFFF	Memory
DSP CD 1	0x90000000 - 0x90000008	Register
DSP CE 2	0xA0000000	Receiver FIFO
DSP CE 3	0xB0000000	Output FIFO

**Registers at the EMIF Bus****5.4.11***Table 5.35: Address Allocation of the Registers*

Register	DSP Select Signal	DSP Address	PCI Local Select Signal	Bit Size Used	R/W Control
Control	CE1	0x9000 0000		9..0	rrrrrw wrrr
Reset	CE1	0x9000 0004		4..0	wwwww
Pipeline	CE1	0x9000 0008	CS1	15..0	r/w all
Information	CE1	0x9000 0020		10..0	rr rrrr rrrr
Debug	CE1	0x9000 0024		10..0	rr

**Format of the Control Register**

The control word makes the differentiated control of the logic functions possible.

CNTR	9000 0000	Control Register	R/W	31-0
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*Table 5.36: Control Register: Bit Fields*

Bits	31..9	8..6	5	4	3	2	1	0
Fields	Not allocated	CALC Error Counter	NG OFF	REC EN	SEND EN	TIME OUT	CALC	INT
Res.	0							

## Description

Table 5.37: Control Register Bit Field Description

Field	Value	Description
INT	0 1	Rising edge detect on NV- value clock. Interrupt. No interrupt.
CALC	0 1	Calculation status of preemphasis. No calculation. Calculation in progress.
TIME OUT	0 1	Time out error of calculation. No time-out. Calculation still in progress at next NV clock.
SEND EN	0 1	Enable or not of sending data to the gradient amplifier. Disabled. Enabled, triggered by each NV clock the DPP sends 1 NG word and a complete set of gradient words out of the FIFO. Exception, no NG word is sent at the first NV clock after SEND EN=1.
REC EN	0 1	Enable or not reading the received gradient data from the gradient controller. Disabled. Enabled.
NG OFF	1	Enables transmitting of FIFO content to the gradient amplifier without NG words if SEND EN=0. Enabled.

## Format of the Reset Register

Table 5.38. Format of the Reset Register

Res_Log	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 = Reset CPLD Logic	NV_SYNC	LVDS Deskew	Preset FIFO OUT	Preset FIFO IN	TIMEOUT	CALC	INT
			0 = Reset Output FIFO				0 = Reset Int.
		0 = Reset LVDS Transmitter				0 = Reset Calculation	
	0 = Reset Next Value synchronisation				0 = Reset Calculation Counter		
				0 = Reset Receiver FIFO			

After initializing the LVDS transmitter it is necessary to reset the input FIFO of the receiving unit.

### Format of the Information Register

Table 5.39: Information Register Bit Fields

<b>Bits</b>	10..6	5	4..0
<b>Fields</b>	PR6 Version	NV Lock	NV Register

Table 5.40: Information Register Bit Field Description

Field	Value	Description
NV Lock	0	Default is 1. Locked. The phase of the NV clock is shifted to the edge of the LVDS clock. Unlocked.
	1	

### Format of the ADR Debug Register

Table 5.41: ADR Debug Register Bit Fields

<b>Bits</b>	10..1	0
<b>Fields</b>	Fixed value	NG_SM_ERR
<b>Res</b>	11 0000 0000	0

Table 5.42: ADR Debug Register Bit Field Description

Field	Value	Description
NG_SM_ERR	0	The phase acquisition NV clock to the LVDS clock is correct. The LV clock edge was not correctly determined.
	1	

### Digital Preemphasis

Digital pre-emphasis means that the digital gradient values given out by the GCU for certain time intervals change the gradient amplifier transfer. The deviating values are determined according to a predefined function and are likewise conveyed to the gradient amplifier.

Digital pre-emphasis is only meaningful when the gradient amplifier evaluates the conveyed values in a fixed, equidistant time period and a valid read has already been received by the DPP for each of these times.

In this case the GCU generates as before the gradient values and the NEXT\_GRADIENT signal. When these values are output they must be adapted to the adjusted gradient raster, which determines the exact time of switching the gradients and the basic values.

Adapted means that the NEXT\_GRADIENT can be flanked at any time between two NEXT\_VALUE, whereby the flank following determines the time of the effectiveness of the gradient packets under summation of a constant pipeline distance.

The minimum gradient raster agreed upon is 1 µsec.

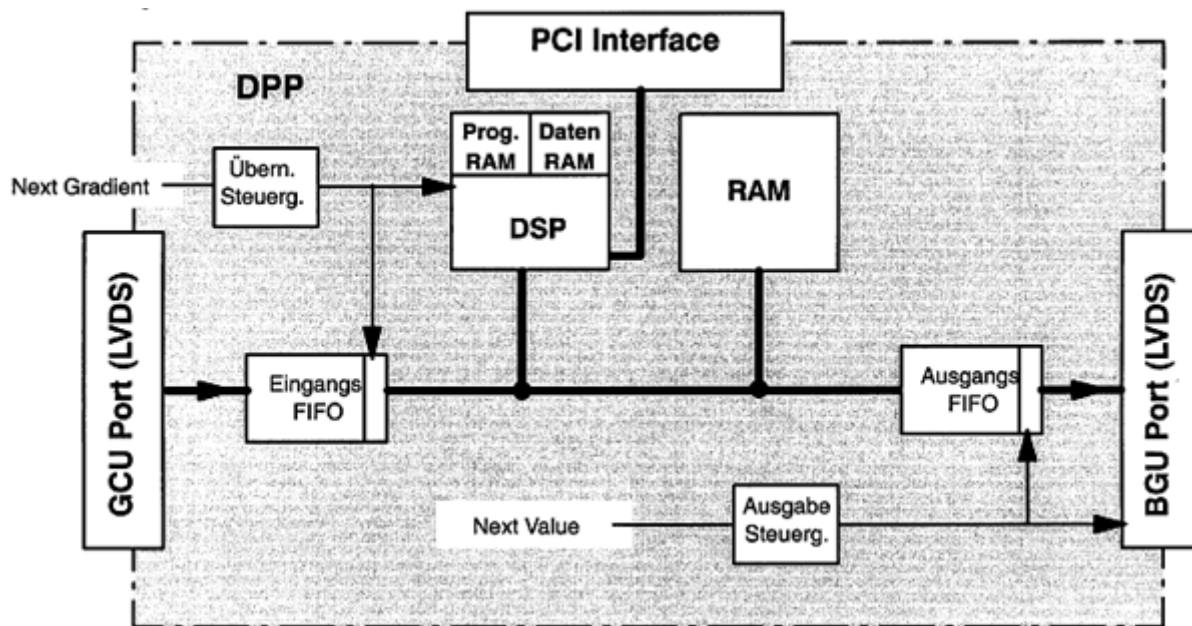


Figure 5.5: Block Diagram

### DPP Pipeline

#### 5.5.1

#### Detailed Procedure

The „NEXT Gradient“ appears before the „NEXT VALUE“. The included gradient packet is transferred directly before or after it, so that the „Next Value“ after next is available at the FIFO output.

Note: „Directly before it“ means after the previous gradient packet belonging to the NEXT Gradient. „Directly after it“ means up to the end of the following „Next Value“ phase.

- The Next Gradient is stored right before the next „Next Value“ flank as „NG flag“. The „NG flag“ is then deleted by the Next Value and stored as „GF“ and „GFD“ until the next „Next Value“. The „GFD“ is read as a status register bit from the DSP in the interrupt service and marked with „logically-1“, the availability of a complete gradient packet in FIFO.
- „GF“ is always set by the „Next Value“ if a stored „NG Flag“ exists. This means with a Next Value phase the GF and GFD remain constant on „1“.

GF:=NF-Flag;  
GFD:=GF;

- Each „Next Value“ sets the INT interrupt signal to the DSP and the CALC bit, which mark the computing phase of the DSP.
- In the interrupt service the DSP reads the status of the GFD, puts the INT bit back as promptly as possible, reads possible gradient words from the input FIFO to the control word, counts and transfers the calculated gradients words and the control word in the output FIFO. As a last action before leaving the service routine, the CALC bit is deleted.
- When the CALC is set the „Next Value“ increments an error counter.
- The control word is the last word of a gradient packet in both FIFO's. With the **DPP1** the control word is transferred with the packet and is used to control the gradient amplifier.

With the **DPP** (48-bit test version) the control word from the out FIFO serves only as a delimiter for the packets and is not transferred with the packet to the gradient amplifier. The reason for this is that the control word in the BGU leads to the deletion of the register.

### **Functional Coordination between the Hardware and Software**

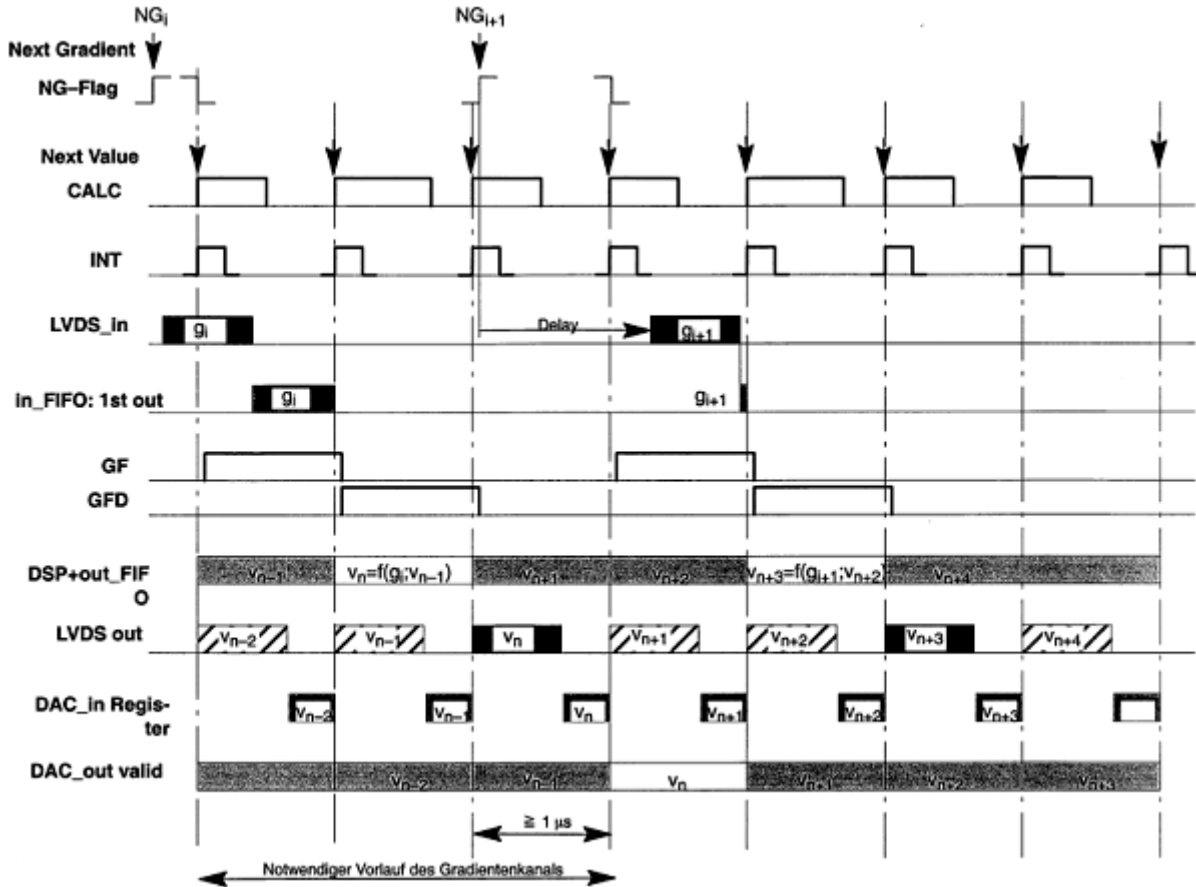
Conditions and software relevant changes when using the DPP:

- In contrast to the case where a DPP is not used, the Next Gradient doesn't switch the gradients, rather determines the Next Value flank, which switches the gradients. In addition the Next Gradient must appear within a certain Next Value phase. The associated gradient packet will then be effective in the fourth phase thereafter!
- The duration between the Next Gradient  $NG_i$  and  $NG_{i+1}$  affects (rounded on whole Next Value phases) the gradients  $g_i$ , when  $g_i$  is the packet that is activated with  $NG_i$ .
- During a Next Value phase only a Next Gradient is given.
- The Next Gradient belonging to the gradient packet must be transferred to the end of the following Next Value phase and must be available at the output of the in\_FIFO.
- It is possible that, for example, all gradient packets are loaded first, to the extent that in\_FIFO can accommodate them. During the experiment the Next Gradients would then only be transferred.
- The transfer sequence of the gradient packets must correspond to the switching sequence specified by the Next Gradient.

## Description

- The number of transferred Next Gradient must be the same or smaller than the number of transferred gradient packets.
- The hardware can suppress a Next Gradient and supply an appropriate error interrupt only when the FIFO contains at least one complete gradient packet.

### **Serial Gradient Cycle, Serial Processing by the DSP**



*Figure 5.6: Gradient Cycle without Parallel Processor*

Figure 5.6: Gradient cycle without parallel processor, „g<sub>i</sub>“ is transferred with maximum delay in a packet with „g<sub>i+1</sub>“ with a maximum delay to the Next Gradient.

**Description**

<b>Next Gradient</b>	The Next Gradient appears before the Next Value that has changed the gradient constant time acquisition. Before or directly afterward the corresponding gradient packet is transferred, that is available at the FIFO output at the Next Value after next. „Before“ means after the previous Next Gradient gradient packet. „directly afterward“ means at the end of the following Next Value phase.
<b>NG-Flag</b>	<p>The Next Gradient is stored right before the next „Next Value“ flank as „NG flag“. The NG flag is overwritten by the Next Value and stored as „GF“ and „GFD“ until the next „Next Value“. The „GFD“ is read as a status register bit from the DSP in the interrupt service and marked with „logically-1“, the availability of a complete gradient packet in FIFO. GF“ is always set by the „Next Value“ if a stored „NG Flag“ exists. This means with a Next Value phase the GF and GFD remain constantly on „1“.</p> <p>GF:=NF-Flag; GFD:=GF</p>
<b>INT, CALC</b>	<p>Each „Next Value“ sets the INT interrupt signal to the DSP and the CALC bit, which mark the computing phase of the DSP.</p> <p>In the interrupt service the DSP reads the status of the GFD, puts the INT bit back as promptly as possible, reads possible gradient words from the input FIFO to the control word, counts and transfers the calculated gradients words and the control word in the output FIFO. Before leaving the service routine, as last action the CALC bit is deleted.</p> <p>When the CALC is set the „Next Value“ increments an error counter.</p>
<b>DSP + out-FIFO</b>	In this phase (when the GFD is set) the DSP reads in a gradient block out of input FIFO, calculates it and writes the value in the out-FIFO.
<b>LVDS out</b>	Reads the output FIFO over the LVDS into the preload register of the DAC's.
<b>Control word</b>	<p>The control word is the last word of a gradient packet in both FIFO's. With the <b>DPP1</b> the control word is transferred with the packet and is used to control the gradient amplifier.</p> <p>With the <b>DPP</b> (48-bit test version) the control word from the out-FIFO serves only as a delimiter for the packets and is not transferred with the packet to the gradient amplifier. The reason for this is that the control word in the BGU leads to the deletion of the register.</p>

# Description

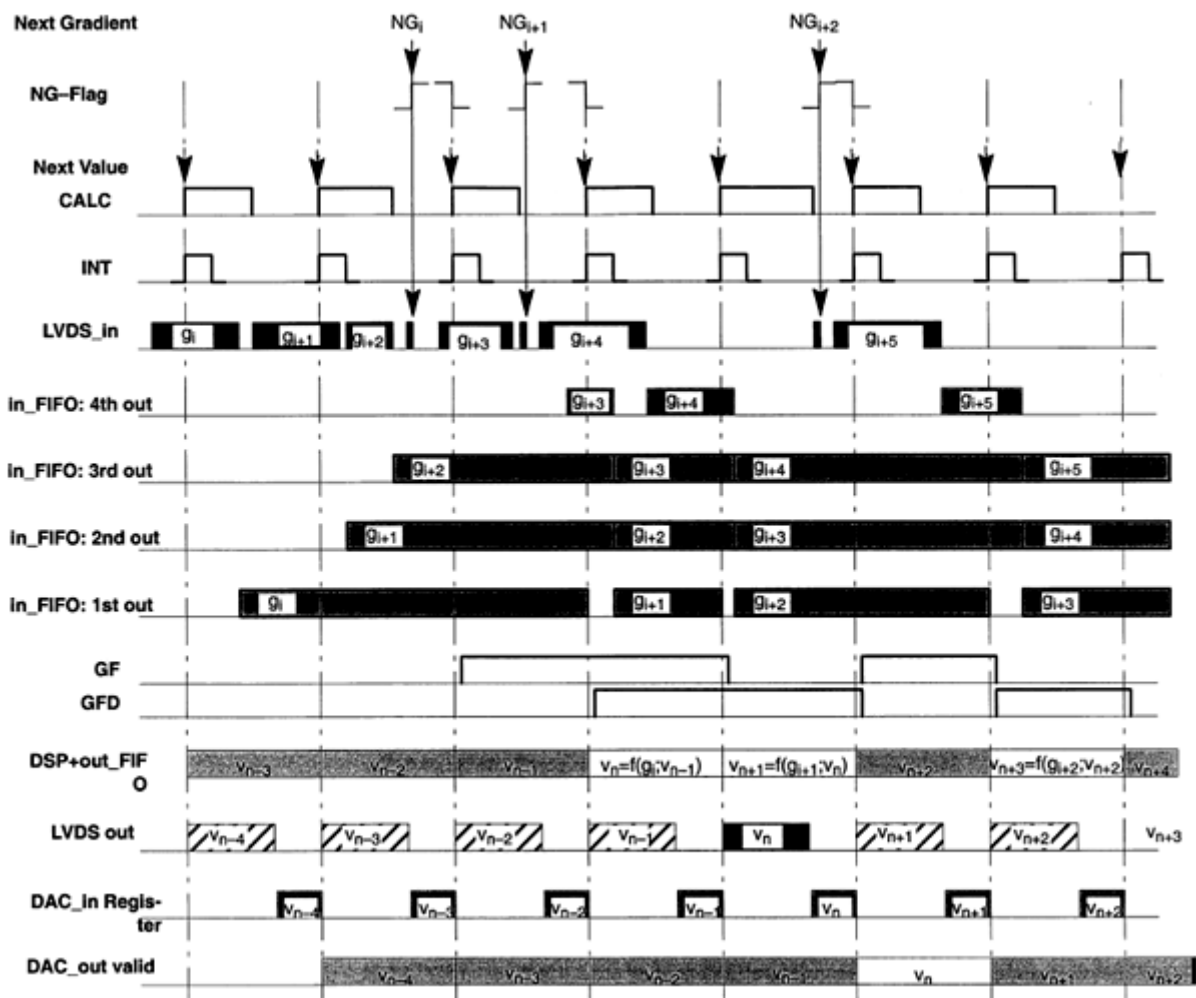


Figure 5.7: Gradient Cycle During Leading Transmission of the Gradients Separately from NG

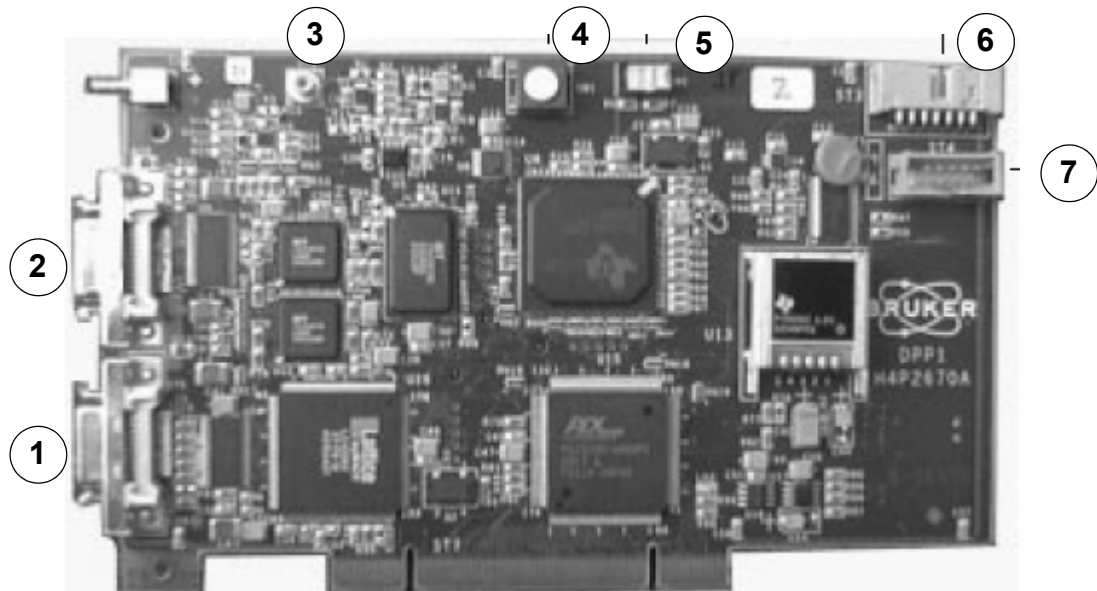
## Description

in-FIFO 1st out

First output line of the FIFO. The DSP reads the gradient block contained in the gaps.

**Dimensions**

Length of the card: Short, 176 mm.



- |                                       |                                    |
|---------------------------------------|------------------------------------|
| 1. INPUT from the Gradient Controller | 5. DSP Emulation Switch            |
| 2. OUTPUT to the Gradient Amplifier   | 6. DSP JTAG Connector              |
| 3. Next Value Clock INPUT             | 7. JTAG Programming/Test Connector |
| 4. Reset Button                       |                                    |

Figure 5.8: IPSO AQS ACQ Built from 5 TX-Controllers

**JTAG Structure**

The board has a JTAG interface with three chains that can be used for programming and testing.

Table 5.43: JTAG Structure on the DPP1

Connector		St4	
JTAG Bridge		U5, Adr=0	
JTAG Chains	<b>Chain1</b>	<b>Chain2</b>	<b>Chain3</b>
	U18, PCI_Controller	U8:DSP	U17:CPLD
Devices			U11:FIFO
			U7:FIFO

**Description**

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**End of Document**

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